

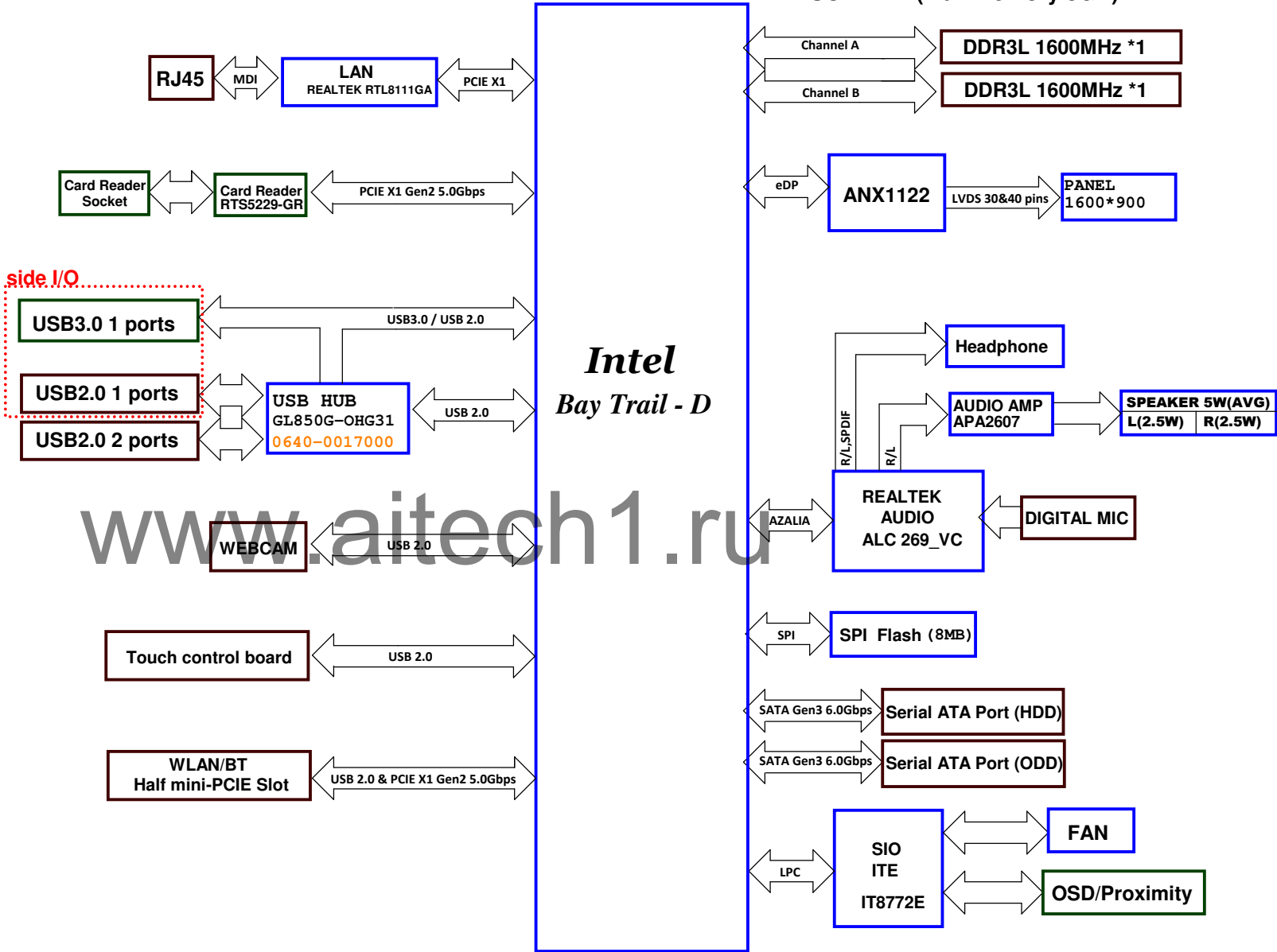
IAXB-T-BL

BERLIN

Revision: 1.02 2014/02/10

PAGE	TITLE
01	BLOCK DIAGRAM
02	POWER ON CHART
03	CHANGE HISTORY 1
04	CHANGE HISTORY 2
05	CHANGE HISTORY 3
06	CHANGE HISTORY 4
07	POWER FLOW
08	POWER SEQUENCE
09	SoC-1 DDR0
10	SoC-2 DDR1
11	SoC-3 Display DDI
12	SoC-4 SATA and PCIE
13	SoC-5 PMU and CLOCKS
14	SoC-6 USB
15	SoC-7 POWER1
16	SoC-8 POWER2
17	SoC-9 VSS
18	SoC De-Cap1
19	SoC De-Cap2
20	VGA
21	DDR3 SO-DIMM 0
22	DDR3 SO-DIMM 1
23	DDR3 TERMINATION A&B
24	eDP LVDS ANX1122
25	DDC CLK DATA SW
26	LVDS CONNECTOR
27	MINI Card-1 (WLAN)
28	REALTEK RTL8111GA
29	LAN Jack
30	Realtek / ALC269_VC
31	AUDIO AMP
32	AUDIO MUTE/CONNECTOR
33	SATA CONNECTOR
34	SIO IT8772E
35	GL850G USB HUB
36	SIDE USB3.0/USB2.0 PORT
37	REAR USB2.0 PORT
38	FAN CONTROLLER
39	FR PANEL/LED
40	reserve
41	WEB CONN&TOUCH CONN
42	RTC/ SPI/ LPC DEBUG
43	CARREADER RTS5229
44	CARREADER Conn.
45	CONVERTER BOARD
46	CONVERTER BOARD SELETCT
47	CURRENT LIMIT
48	DC IN UVP OVP &19VSB**0401
49	5VSB 3P3VSB
50	1P0VSB &1P8VSB
51	12V
52	19V 3P3V 5V 1P2V 5VDUAL
53	+1P35V DUAL&+VTT DDR
54	Vcore Controller
55	+Vcore & +VNN Output MLCC
56	1P0V 1P05V
57	1P35V 1P5V 1P8V
58	3P3V SOC
59	LEVEL SHIFT CIRCUIT& STRAP_1
60	LEVEL SHIFT CIRCUIT& STRAP_2
61	LEVEL SHIFT CIRCUIT& STRAP_3

62	LEVEL SHIFT CIRCUIT& STRAP_4
63	LEVEL SHIFT CIRCUIT& STRAP_5
64	LEVEL SHIFT CIRCUIT& STRAP_6
65	Test Point
66	XDP PART
67	DISCHARGE



Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

Property: BOM
I = Installed Part.
NI = Not Installed Part.
PROTO = PROTO Phase Only.
VP = Virtual Part.
NOBOM = Symbol only.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON

Title : BLOCK DIAGRAM

Pegatron Corp.

Engineer: Wade_Pan

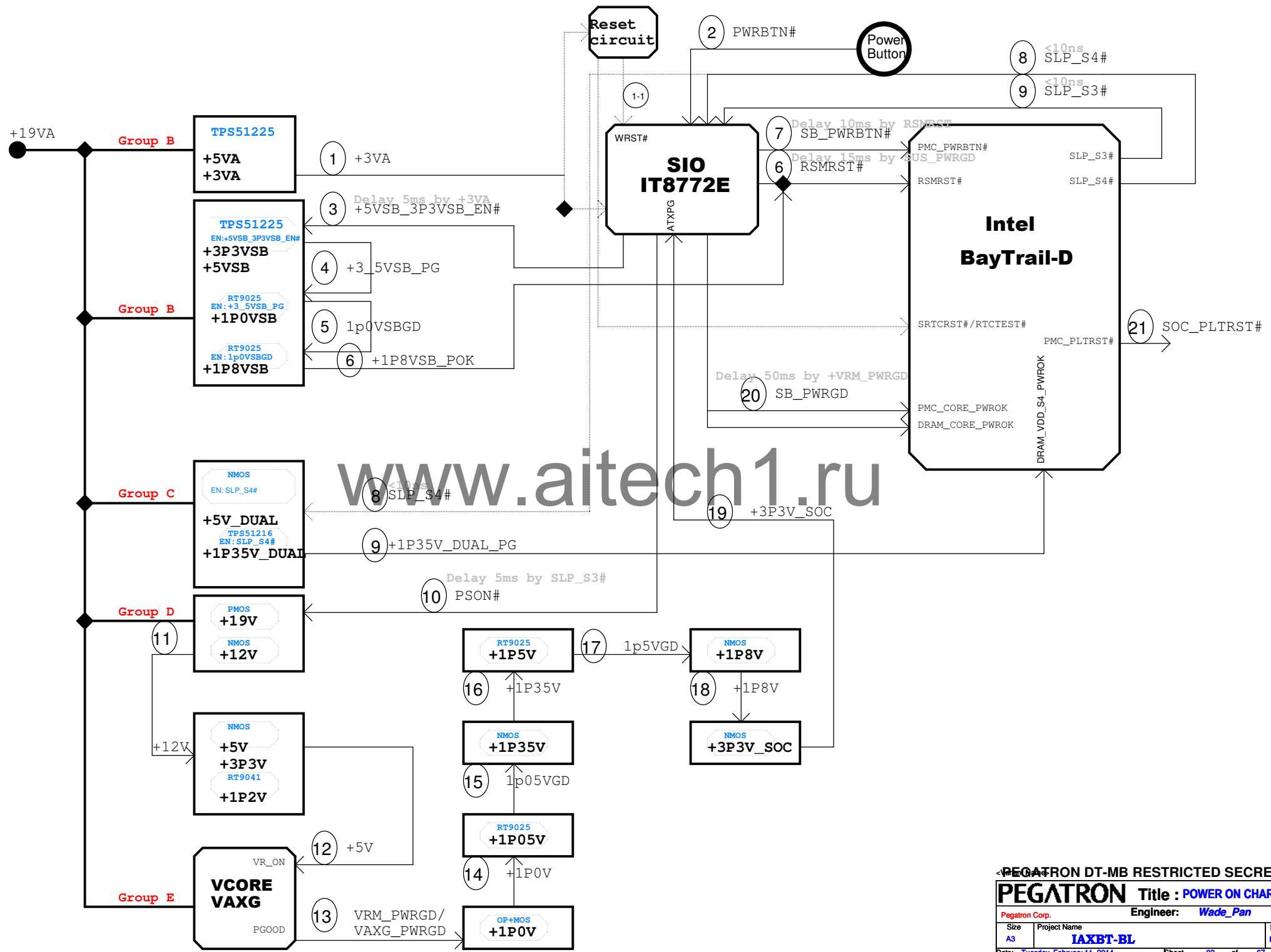
Size A3

Project Name IAXB-T-BL

Rev R1.01

Date: Tuesday, February 11, 2014

Sheet 01 of 67



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09.Soc-1 DDR0
(12/11)
# C01 from 0.1uF/Ni to 330pF/Ni
# C02 from 0.1uF/I to 330pF/I
(12/13)
# C01 from Ni to I

11.Soc-3 Display DDI
(12/16)
# DEL SM_TP408
# DEL SM_TP407
# R44 from 2.2K to 1K
(12/16)
# R44 change to small
(12/17)
# R89, R92, R93 from I to PVT_NI

12.Soc-4 SATA and PCIe
(11/28)
# R21 from 10K to 1K
(12/11)
# AR2~AR5 from 33ohm to 22ohm
(AZ_RST#, SYNC, BITCLK, SDATA_OUT)
(12/14)
# add LC43_NI for critical noise tuning
(1/7)
# LC43 from 0.1uF to 330pF
(1/12)
# DEL SM_TP213

13.Soc-5 PMU and CLOCKS
# [U1.B16] from TP to net(GP_DDR_Vref)
# [U1.C18] from floating to net(OVER_CURRENT#)
# [U1.A17] from TP to net(LPC_PME#)
# [U1.AV32] from floating to net(UMA_DDC_DAT_W)
# [U1.BA28] from floating to net(UMA_DDC_CLK_W)
# [U1.AY28] from floating to net(DDC_DATA_CLK_SW)
(10/29)
# R74 from Ni to I, XDP_NI
(11/5)
# SC8, SC9 from 18pF to 10pF
(12/2)
# HCB32, HCB27 from Ni to I_330pF
(12/15)
# SC34, HCB29, HCB28, SC9, HCB36, R100, R101,
R124, R103, R123, R383 change to small
# R24, R27, R28, R121, R118 change to short pin
(12/16)
# DEL HCB36, SM_TP509
# JP30, JP32(R27, R28) change to short directly
(12/24)
# HCB28 from 0.1uF_NI to 330pF_I
(12/27)
# R75, R76, R77 from 22 ohm to 0 ohm for EA issue
(1/7)
# add HCB35_NI for SYS_RESET#
# HCB29_I from RTCTEST# to SRTCRST#
(1/12)
# DEL SM_TP512, SM_TP513
(01/28)
# SC34 from Ni to 330pF_I
(02/10)
# SC34 from 330pF to 100pF
# HCB35 from Ni to 330pF I

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Size A3	Project Name IAXBT-BL	Rev R1.01	
Date: Tuesday, February 11, 2014	Sheet 03 of 67		

Schematics Change History

27.MINI Card-1 (WLAN)
(10/23)
DEL net name "3.3VAUX";
WLC5 from 0.1uF/16V_I to 1uF/6.3V_I
WLC2 from 0.01uF/25V_I to 1uF/6.3V_I
WLC3 from 1uF/6.3V_NI to 1uF/6.3V_I
add AR143 between +3P3VSB and +3V_WLAN
DEL: WLR2, WLR6, WLR7, WLR8
DEL net name: 3V_WLAN_2[J60.39], 3V_WLAN_1[J60.41]
(10/23)
DEL net name "RESERVED3", "RESERVED6"
WLC5 from 1uF/6.3V_I to 0.1uF/6.3V_I(0402)
WLC2 from 1uF/6.3V_I to 0.1uF/6.3V_I(0402)
WLC3 from 1uF/6.3V_I to 0.1uF/6.3V_I(0402)
(12/2)
WLC13 from NI to I_330pF
(12/15)
WLR3, AR143 change to short pin
(12/17)
add JP67

28.REALTEK RTL8111GA
add R408
[LU1A.19] from PCIRST1#(SIO_main) to PCIRST3#(SIO_SB)
(10/22)
DEL net name "RL_LAN_TXN_C" on [LU1.14]
DEL net name "RL_LAN_TXP_C" on [LU1.13]
(10/23)
LR6 from 15K 5% to 15K 1% (merge)
(12/15)
R408 change to short pin

29.LAN Jack
(12/16)
DEL UU10, UU11

30.Realtek / ALC269_VC
DEL: D3, D4, D10, D11, Q99, AR115, ACB28,
R235, AR116, C122, ACB30, R144, AD11, AR16
C18, C25, C28, C32 from 0805 to 0603
C34, C36 from I to NI
add C321, R425
C48 mirror horizontally
(10/22)
change net name connect to ACE22, ACE21
DEL net name "+3VS_CODECC" on [U9477.1]
D6 from I to NI
(10/23)
AR21 from short pin to 0 ohm
(12/11)
R140 from 33ohm to 22ohm (AZ_SDATA_IN)
(12/15)
R67, R425 change to short pin
(12/16)
JP42(R425) change to short directly

31.AUDIO AMP
AR53 from 120K to 10K
add AR31 pull high +3P3V and AR138 Pull down
connect to [AU3.21]
AR132, AR133 from 10K to 5.23K; AR135, AR134 from
10K to 1K; AR136, AR137 from 10K to 845 ohm
AD6, AD7, AD8, AD9 from I to NI
DEL: D104
(10/22)
AR138 from 10K to 0 ohm
AR40 from short pin to 0 ohm
add AC84(place near [AR40.1])
(10/23)
AR66 from 10K to 15K
AR131 from short pin to 0 ohm

31.AUDIO AMP
(12/2)
AC76, AC78 change to 0.1uF for 480MHz radiation
(12/11)
AD6, AD7, AD8, AD9 from NI to I
(12/15)
AR40 change to short pin
(12/16)
AR132, AR133 from 5.23K to 8.06K
AR136, AR137 from 845ohm to 887ohm
(1/6)
AL7, AL10, AL11, AL14 change to 0805 30ohm bead
for EMI issue
(1/10)
add short pin "JP69"

32.AUDIO MUTE/CONNECTOR
add AR141, AR140 and connect [AR141.1], [AR123.1],
[AR19.1] to +3P3VA; [AR140.1], [AR122.1] to +3P3V
DEL: AQ7, AR124
Mute_CTL# connect to SIO[02U1.37]
(10/22)
AR18 from I to NI
add PQ457_NI, R437_I, AR142_NI pull high to +3P3VA, AR18_NI
(12/26)
J76 package type from "DIP" to "SMD"

33.SATA CONNECTOR
(11/15)
DEL: Tc18
(12/26)
P306 package type from "SMD" to "DIP"
(01/28)
P67 should change P/N to "1208-01NE000" through ECN

34.SIO IT8772E
DEL: R395, T89, T88
add O2C28
change D103 part from one diode to two diode
add [O2U1.10], [O2U1.42], [O2U1.60] pull high R.
(O2R176, O2R177, O2R179)
connect [O2U1.58] to PLED1
O2R10 from I to NI
[O2R20.1] from +3P3VSB to +1P8VSB
connect [O2R20.2] to [U1.A17]
O2R79 from 4.7K to 1K
(10/21)
O2R176 from +3P3V to +3P3VSB
(10/22)
add O2R180 pull high to +5VA
(10/29)
O2R23 from 10K to 1K
O2R171 from NI to I
(11/8)
R32 from 0 ohm to 12 ohm
(11/19)
OSC1 from 50ppm to 25ppm
O2C28 from 0.1uF to 0.01uF
(12/11)
add SQ2 for EA solution
(12/14)
add O2C29 for critical noise tuning
(12/15)
DEL SR100~SR104
(12/17)
O2C11 from 1uF/50V/0603 to 1uF/16V/0603
O2C29 change to 1000pF_I
(12/24)
O2C29 change to NI
(1/13)
add R453, R454, R455, R456, R457
O2R175 change to I
D103 change to NI

35. GL850G USB HUB
(12/14)
DEC35 change to small symbol
(12/15)
R158 change to short pin
(12/16)
JP44(R158) change to short directly

36.SIDE USB3.0/USB2.0 PORT
UR131, UR132, UR1 from I to NI
[UR131.2] connect to [U1.J3] through level shift
[UR132.2], [UR1.2] connect to [U1.H3] through
level shift
(11/28)
change USB2 mx_P/N, from 12X130721000 to
12X05714B050
(12/2)
URN51, URN50 from I to NI
UL22, UL23 from NI to I
(12/15)
URN52 change to short pin
(12/16)
DEL UL24
JP45, JP46(URN52) change to short pin directly

37.REAR USB2.0 PORT
(12/2)
URN36, URN37 from I to NI
UL3, UL4 from NI to I

38.FAN CONTROLLER
CFAN_PWM_R add FD2(NI) to +3P3V
CPUFAN_TACH_R add FR9(NI) to +3P3V
(10/29)
D102 from BAW56 to BAT54

39.FR PANEL/LED
(10/22)
CR1, CR2, R7, R8 from I to NI
(12/11)
O3C1 from 0.1uF to 1000pF
(12/18)
R7, R8, CR2, CR1 change to "I, MP_NI"

41.WEB CONN&TOUCH CONN
(12/15)
URN53, RN3 change to short pin
(12/16)
DEL UL25, L110
JP47, JP48, JP49, JP50(URN53, RN3) change to
short pin directly

42.RTC/ SPI/ LPC DEBUG
(10/22)
F3C1 from I to NI
IU1 from SMD to DIP
(10/23)
add net name "LAD0_RR", "LAD1_RR", "LAD2_RR",
"LAD3_RR", "LFRAME#_RR", "LPCCLK[1]_25MHz_RR"
(11/8)
R50 from 0 ohm to 12 ohm
(11/14)
change SPI debug header(from 2x4 to 2x5) and jumper
(12/15)
BR2, BR3, BR4, BR5 change to small
BC1, BC2, BC3 from 1uF/16V/0603 to
1uF/6.3V/0402/small

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PEGATRON		Title : CHANGE HISTORY	
Pegatron Corp.		Engineer: Wade_Pan	
Size A3	Project Name IAXBT-BL	Rev R1.01	
Date: Tuesday, February 11, 2014 Sheet 04 of 67			

42.RTC/ SPI/ LPC DEBUG
(12/17)
F3R2 from 1K_NI to 0_NI
(12/17)
IU2 change to "I, MP_NI"
(12/26)
IU1 package type from "DIP" to "SMD"
(12/27)
F3R1 from 10 ohm to 22 ohm for EA issue

43.CARREADER RTS5229
add CRR35
DEL: CRC1, CRC2
[U9481.23] from PLTRST#
(SOC level shift) to PCIRST1#(SIO_main)
(12/15)
CRR8, CRR35, CRR34 change to short pin
(12/17)
add JP68
JP52, JP53(CRR35, CRR34) change to short directly

44.CARREADER Conn.
(10/22)
OP1C2 from NI to I

45.CONVERTER BOARD
connect PSEL_1 to [O2U1.62] and change pull high
from NI to I
connect PSEL_0 to [O2U1.64] and change pull high
from NI to I
(12/17)
PR79, PR80, PR6, PR78, PJ3, PD12, PD13 change to NI
(01/10)
PC27 from 0.1uF/0603/25V to 0.1uF/0402/25V

46.CONVERTER BOARD SELETCT
(10/23)
add PR616(place near AC48)
PR51 from I to NI
(12/17)
PD6 change to NI

47.CURRENT LIMIT
add R423(0 ohm) and pull high R(O2R178) to [U1.C18]
(10/21)
net name "OVER CURRENT#" change to "OVER_CURRENT#"

48.DC_IN UVP OVP &19VSB**0401
change PQ2 to another P/N
(12/26)
PJ1 package type from "DIP" to "SMD"

49.5VSB_3P3VSB
PQ17 from MOS to BJT, and add R433 connect to net
(+5VSB_3P3VSB_EN#)
PC41, PC43 from 0805 to 0402
(10/29)
R433 from 1K to 10K
(12/15)
PR128, PR72, PR112, PR153 change to short pin

50.1P0VSB &1P8VSB
[PU3.4], [PU5.4] add net name
PC357, PC380, PC104, PC102 from 0805 to 0402
(11/27)
add PR617 for EA sequence
(01/28)
PR93 from 12.7K to 13K

52.19V_3P3V_5V_1P2V_5VDUAL
DEL: PC17, PQ6, PQ5, PR41
add PR613, PR614, PR615 and modify circuit
[PU4.1] add net name, [PU4.3] change net name

52.19V_3P3V_5V_1P2V_5VDUAL
(10/23)
change net name from "1P8VSB_ADJ" to "1P2V_ADJ"
(12/13)
PC111 from 0.1uF(0402) to 1uF(0603)

53.+1P35V_DUAL&+VTT_DDR
(10/21)
add R434
(10/23)
PR39 from 100K to 200K
PR143 from 30K to 49.9K
(11/22)
PR138 from 52.3K to 29.4K for OCP change
(12/11)
merge PC153, PC154 from 10uF/25V/1206/bottom *2
to PC153/22uF/25V/0805/Top *1
(12/16)
PR39 from I to NI
(01/28)
PR142 from 75K to 88.7K

54.Vcore Controller
(10/23)
PR234 from 20 ohm(0603) to 20 ohm (0402)
PR241 from 309K to 316 ohm
(11/8)
PR215 from 2.43K to 2.67K (for load line)
PR196 from 2.43K to 2.61K (for load line)
(11/19)
PC370 from 0.22uF(0603) to 0.1uF(0402)
for Vcore transient
PR228 from 301 ohm to 976 ohm
for Vcore transient
PR215 from 2.67K ohm to 2.55K ohm
for Vcore transient
PL9 from 0.36UH/60A to 0.47UH/17.5A
for Vcore transient
PC173 from 0.22uF(0603) to 0.1uF(0402)
for VAXG transient
PR241 from 316 ohm to 1.02K ohm
for VAXG transient
PR193 from 24.9K ohm to 21K ohm
for VAXG transient
PR196 from 2.61K ohm to 2.32K ohm
for VAXG transient
PL10 from 0.36UH/60A to 0.47UH/17.5A
for VAXG transient
(12/4)
PR175 form 1ohm/0603/1% to 2.2ohm/0805/5%
(12/15)
PR606 change to short pin
(01/13)
PR215 from 2.55K to 2.21K

56.1P0V_1P05V
[PU2.4] add net name
#PC85, PC87 from 0805 to 0402
(10/23)
PC23, PC20, PC22 from 10uF/10V to 10uF/6.3V
(11/5)
PR158 from 10K_5% to 10K_1%
(12/11)
PR70 from 10K to 10.5K
(12/14)
add C324 for critical noise tuning
(12/17)
PR160, PR609 from 0ohm to 402ohm
PR610 from 1K to 10K
(01/28)
PR156 from 22.6K to 22.1K

57.1P35V_1P5V_1P8V
[PU92.4] add net name
PC98, PC99 from 0805 to 0402

59.LEVEL SHIFT CIRCUIT& STRAP_1
add GU5, C322, R410; [GU5.5] connect
to +3P3VSB and [GU5.4] connect to net(PCIRST2#)
(12/11)
add R441 for EA solution
(01/10)
add C325_NI
(01/13)
add R451
(01/28)
C98, R165, Q3, Q4 from NI to I
R384 from I to NI
(2/6)
C98 from I to NI

60.LEVEL SHIFT CIRCUIT& STRAP_2
(10/23)
R184 from 10K to 4.7K
(10/29)
R184 from 1% to 5%

61.LEVEL SHIFT CIRCUIT& STRAP_3
(10/29)
add Q108, R438, R439 for level shift of PCIRST#
(11/27)
R439 connect from +3p3v to +3p3vsv
add R440

62.LEVEL SHIFT CIRCUIT& STRAP_4
DEL: Q22, Q23, R208, R209
add level shift for USB2_EN(Q106, R427,R428, R429)
add level shift for USB3_EN(Q107, R430,R431, R432)
(10/23)
R37 from 3K to 15K
R33 from 2K to 10K
(10/29)
U9522 from 06X900827000 to 06X900957000
(12/15)
R429, R432, R216 change to short pin
(12/16)
add R442, SOC_INT_SERIRQ pull high R
(1/12)
R37 from 15K to 10K
R33 from 10K to 15K

63.LEVEL SHIFT CIRCUIT& STRAP_5
add O2Q3, O2Q4, R421, R422, R419, R420, R414, R413, R412
for thermal sensor
(10/22)
[O2Q1.2] from "SIO_VR_TSD-" to "SIO_VR_TSD1-"
[O2Q2.2] from "SIO_MB_TSD-" to "SIO_MB_TSD1-"
[O2Q4.2] from "SIO_VR_TSD-" to "SIO_VR_TSD2-"
[O2Q3.2] from "SIO_VR_TSD-" to "SIO_MB_TSD2-"
(10/22)
add JP23(place near SIO)
change name from JE60:13 to JE61:12
(12/14)
R412, R414 from I to NI
R420, R422 from NI to I
(12/15)
HOTR2 change to short pin
(12/16)
R411, R413, R420, R422 change to short pin
(12/17)
O2Q1, O2Q3 change to NI

<Variant Name>

PEGATRON		Title : CHANGE HISTORY	
Pegatron Corp.		Engineer: Wade_Pan	
Size A3	Project Name IAXBT-BL		Rev R1.01
Date: Tuesday, February 11, 2014		Sheet 05	of 67

Schematics Change History

64.LEVEL SHIFT CIRCUIT& STRAP_6
add level shift for DDC_DATA,
I2C_DATA(U9526, R392, R390, R393,
R394, R391, R401, R404, R402, R403,
C121, C120, C117, C118, C119)
add level shift for DDC_CLK_DATA_SW
(Q104, R405, R406, R407)
(10/21)
[R159.1], [R160.1], [R161.1] from
+3P3V to +1P8V
R410 from I to NI
(12/16)
R227, R228, R229, R230, R231, U9491, C108,
C110 change to "DVT_NI"
(12/17)
Q104, R405, R406, R407 from "I" to "DVT_NI"
R403, R404, R390, R393, R392, R394, R391, C120,
C118, U9526 from "I" to "DVT_NI"
R160,R159 change to NI
SR308, SR61 from "I" to "DVT_NI"
(1/7)
U9491, U9526 change package
(1/10)
DEL R402, R401 and I2C signal
add Q109, Q110
(1/13)
add R444, R446, R450, R448

65.Test Point
(10/23)
U9482 change P/N
(1/5)
DEL U9482 (label)

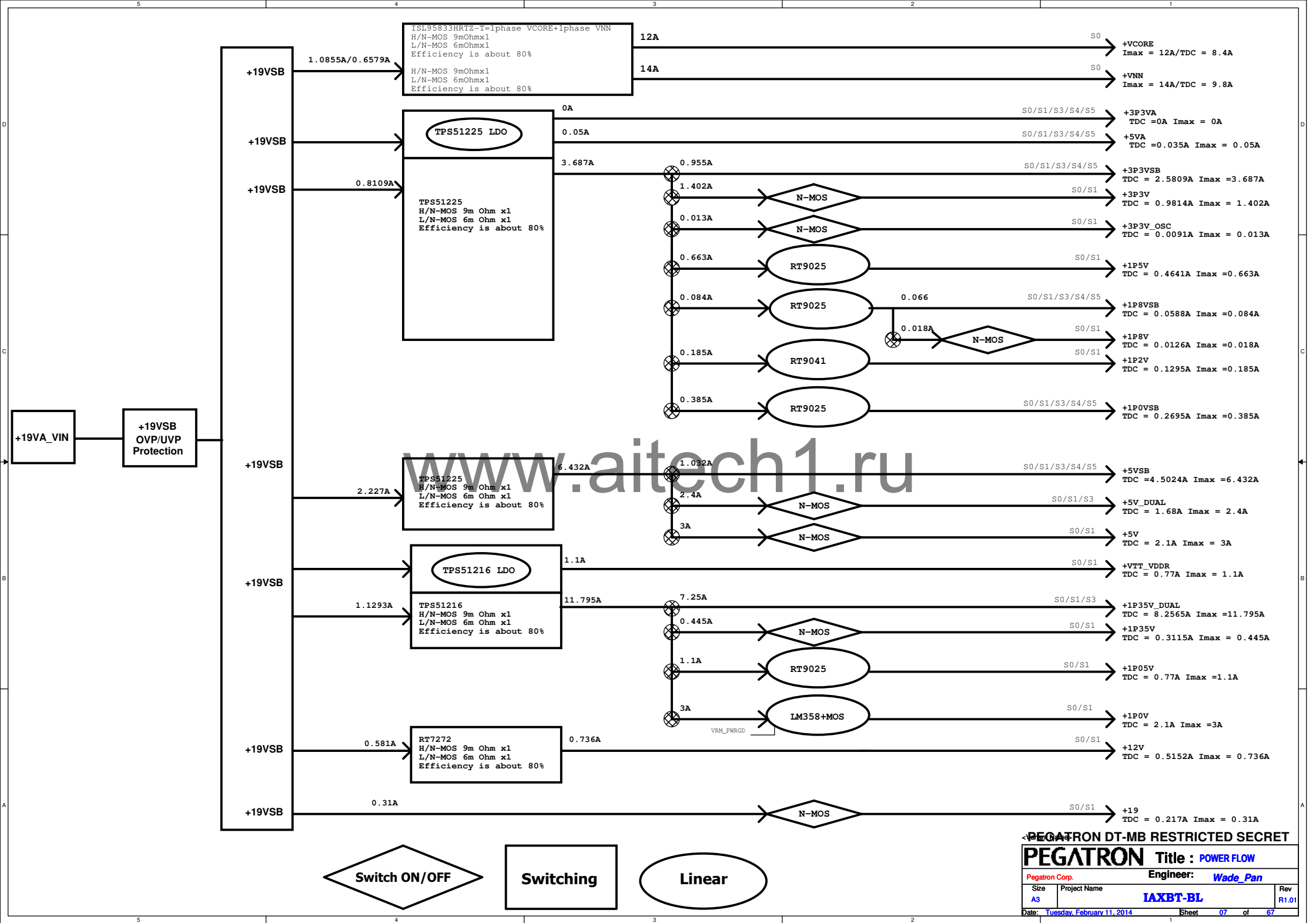
66.XDP PART
[XDP1.43] connect to +1P8VSB;
[XDP1.44] connect to +1P8V
(12/17)
change XDP1 PCB footprint to "nsp" type
(12/24)
change back XDP1 PCB footprint and change
to "NI, XDP_I"
(1/12)
change XDP1 PCB footprint to "nsp"

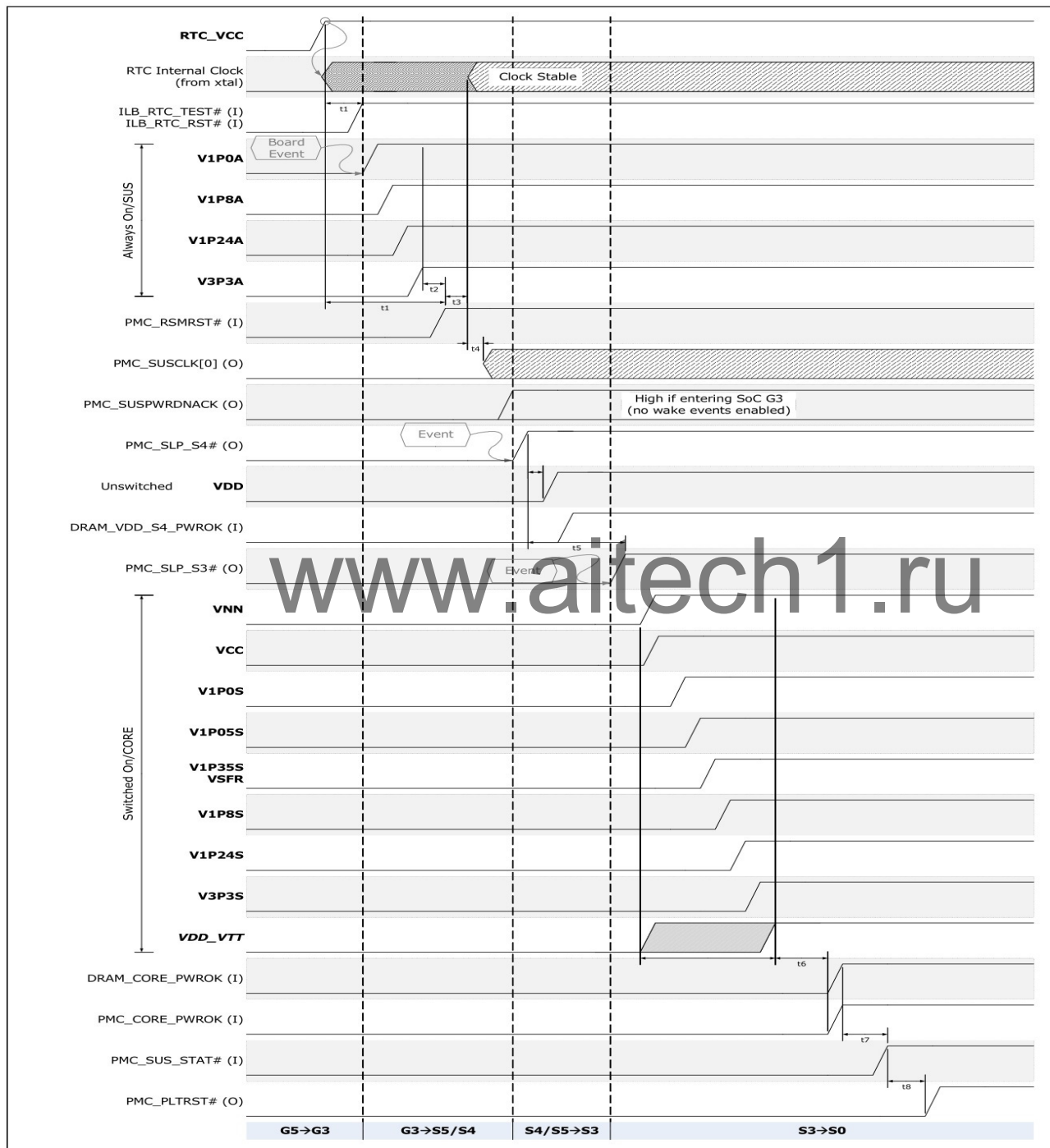
67.DISCHARGE
DEL net name "PQ9515_D"

Schematics Change History: for BOM merge

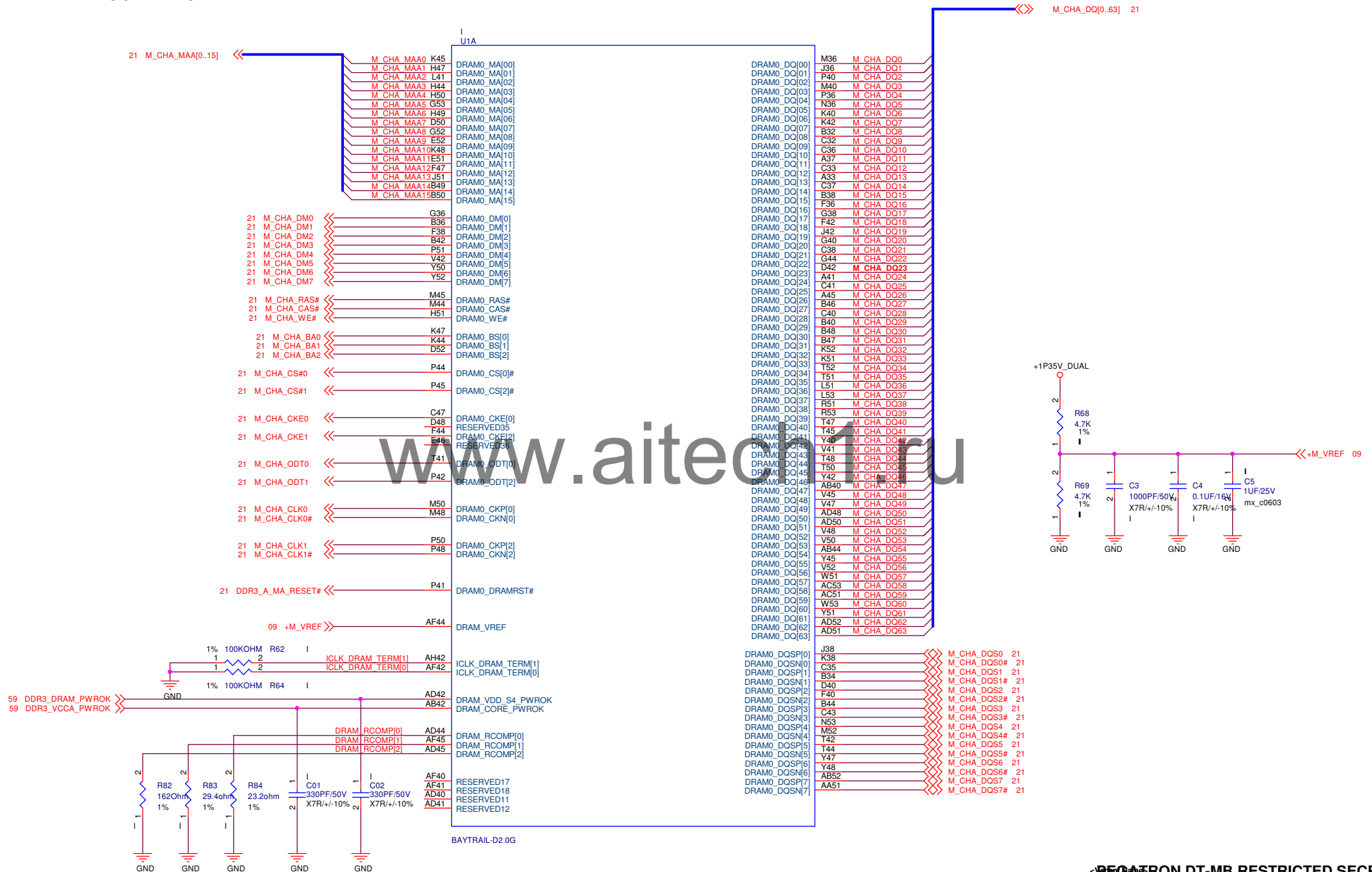
(12/30)
FERRITE BEAD (0805)180OHM/2A (L1,L2,L3,L4,L5,L27) merge to FERRITE BEAD (0805) 3A 70 OHM
100ohm/0402/5% (LR56,LR57) merge to 100ohm/0402/1%
10.5K/0402/1% (PR70) merge to 10K/0402/1%
100K/0402/5% (PR133,PR135,PR249,PR256,R43,R91,R124,R125,VR4,VR5) merge to 100K/0402/1%
20K/0402/5% (PR81) merge to 20K/0402/1%
22K/0402/5% (PR45,PR58) merge to 22.6K/0402/1%
30ohm/0402/5% (PR44,PR54) merge to 29.4ohm/0402/1%
33ohm/0402/5% (O3R8,O3R5) merge to 29.4ohm/0402/1%
29.4K/0402/1% (PR138) merge to 30K/0402/1%
30.1K/0402/1% (AR30,AR31) merge to 30K/0402/1%
32.4K/0402/1% (PR69) merge to 30K/0402/1%
37.4K/0402/1% (PR77) merge to 39.2K/0402/1%
39K/0402/1% (PR264) merge to 39.2K/0402/1%
47.5K/0402/1% (PR106) merge to 47K/0402/1%
51ohm/0402/5% (R73,R100,R101,R102,R103) merge to 49.9 ohm/0402/1%
510ohm/0402/1% (R138) merge to 499ohm/0402/1%
69.8K/0402/1% (PR47) merge to 75K/0402/1%
8.2K/0402/5% (PR208,PR210,PR214,PR243,PR245,PR266,F3R5,F3R11,PR60,PR111,PR127) merge to 8.2K/0402/1%
(12/31)
0.1uF/0402/6.3v/X5R (DEC21,DEC50,DEC86,DEC126,DEC132,DEC133,DEC134,DEC135,WLC2,WLC3,WLC5) merge to 0.1uF/0402/16v/X7R
0.1uF/0402/25v/X7R (PC157,PC184) merge to 0.1uF/0402/25v/X5R
2.2uF/0603/6.3v (DEC4,DEC5) merge to 2.2uF/0603/16v
0.22uF/0603/10v (PC139) merge to 0.22uF/0603/25v

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SODIMMO

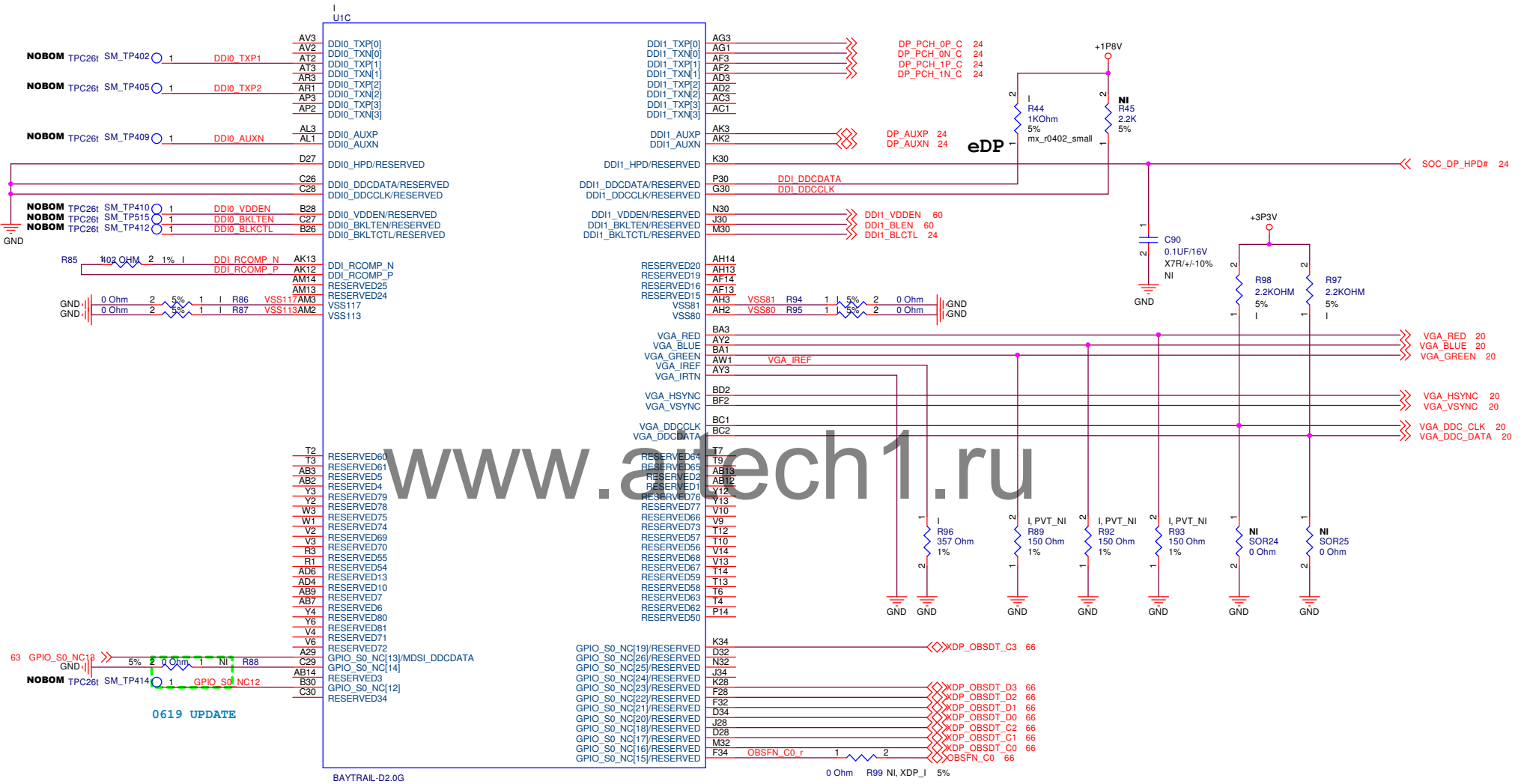


22 M CHB MAB[0..15]

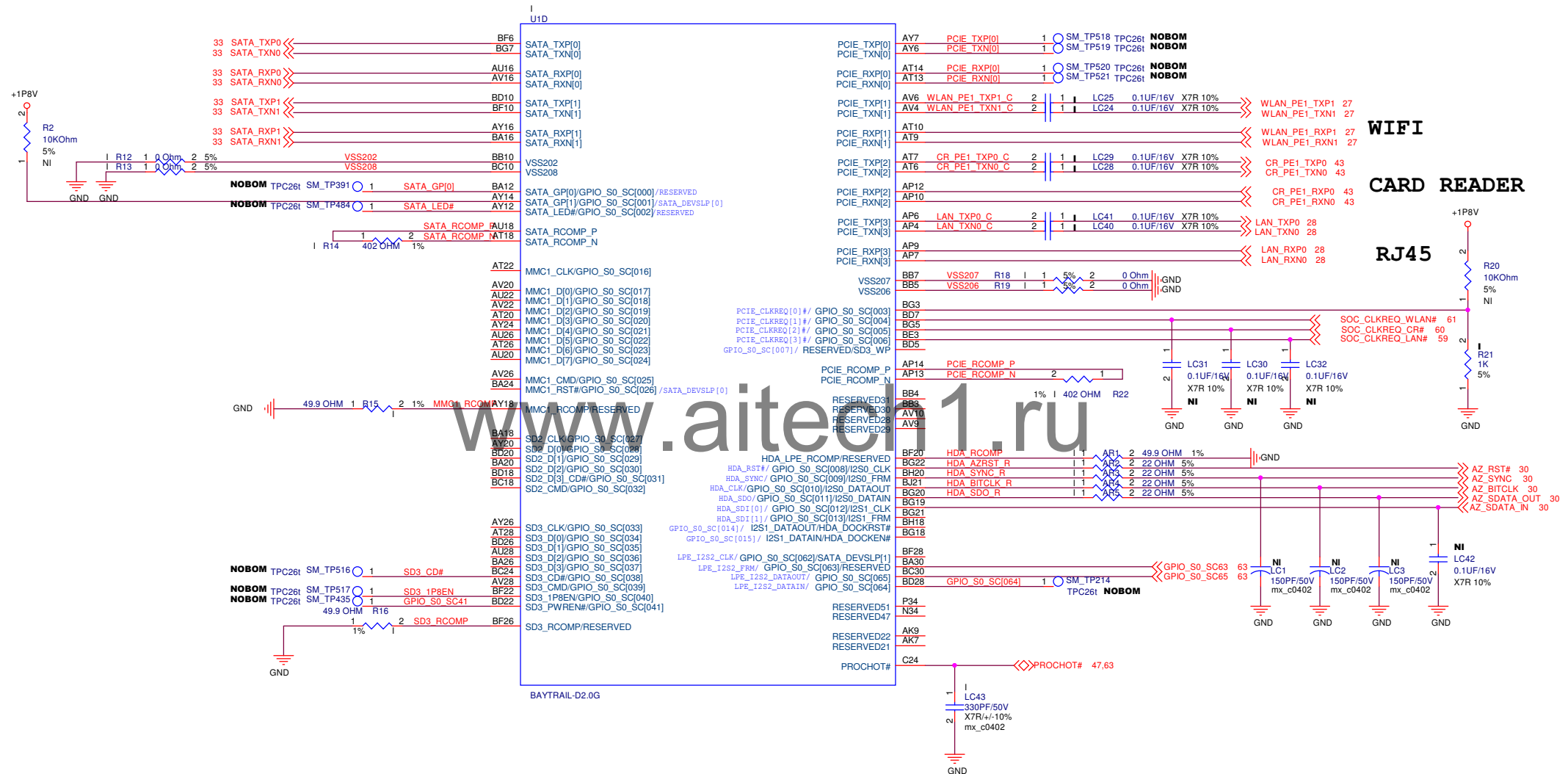


Date: Tuesday, February 11, 2014 Sheet 10 of 67

Berlin DISPLAY



SATA AND PCIe



<Verbatim Name> REGATRON DT-MB RESTRICTED SECRET

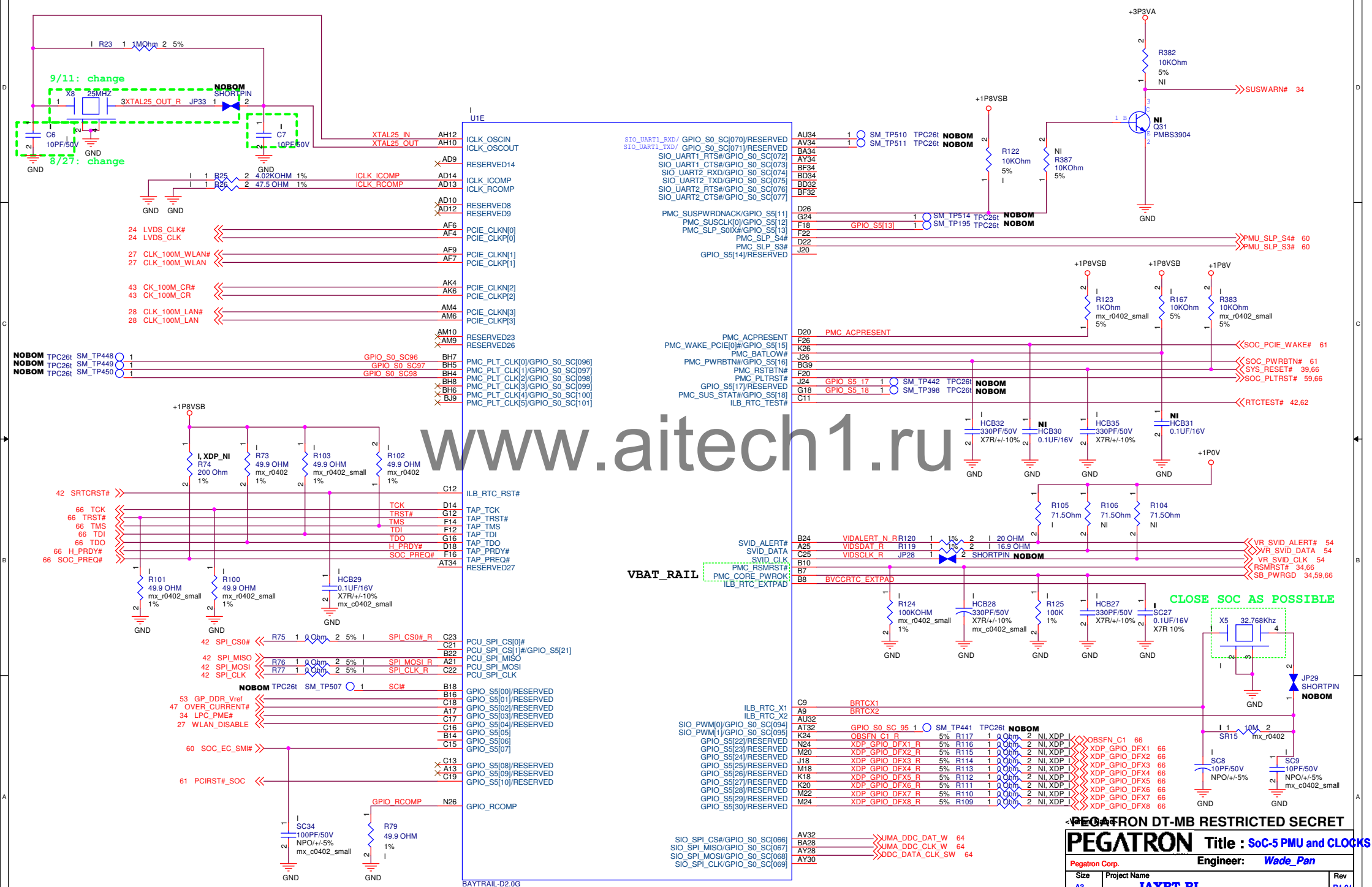
PEGATRON Title : SoC-4 SATA and PCIe

Pegatron Corp. Engineer: *Wade_Pan*

Size	Project Name	Rev
A3	IAVPT RI	R1.01

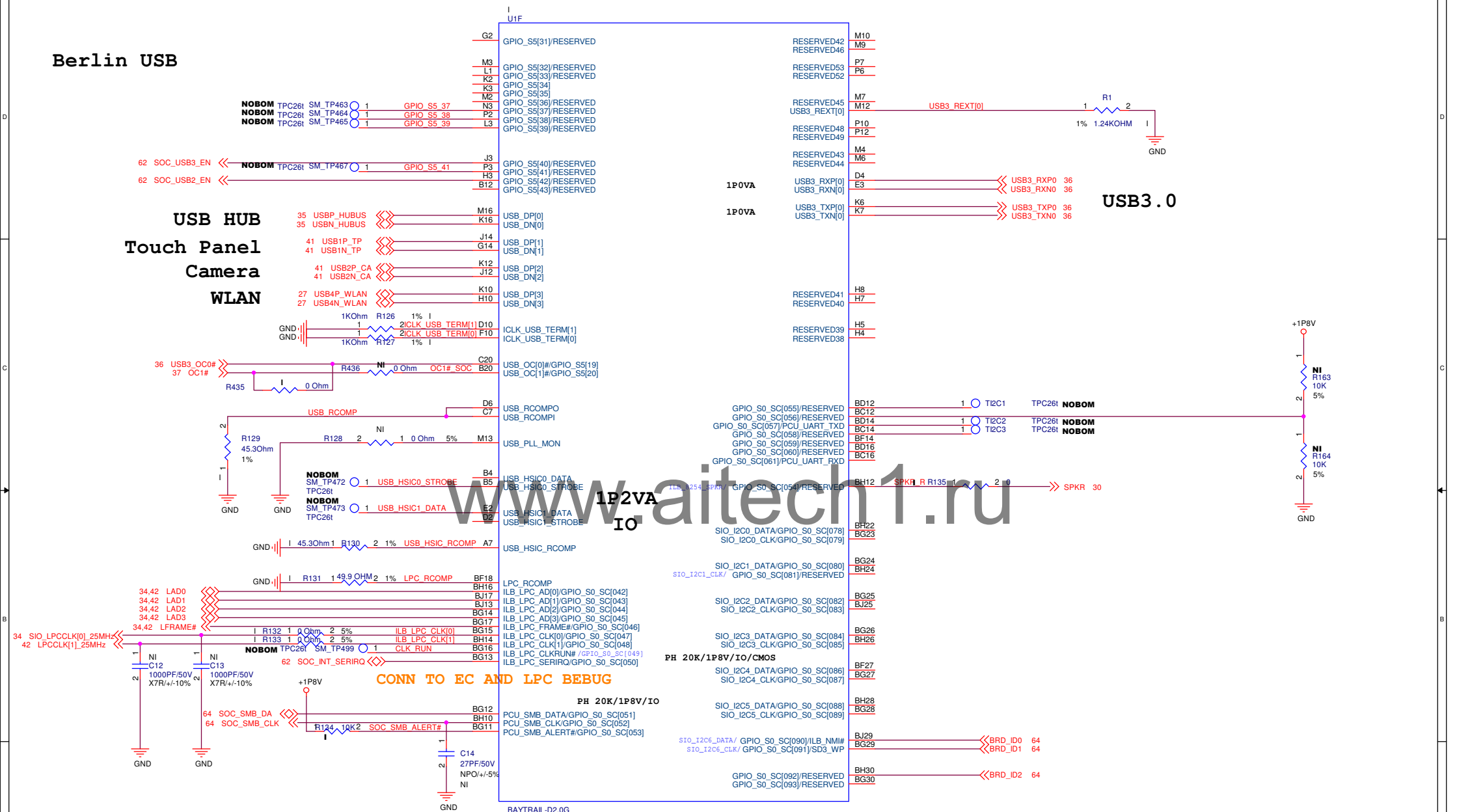
A3	IAABT-BL	R1.01
Date: Tuesday, February 11, 2014		Sheet 12 of 67

Berlin PMU & CLK



< PEGATRON DT-MB RESTRICTED SECRET			
PEGATRON		Title : SoC-5 PMU and CLOCKS	
Pegatron Corp.		Engineer: Wade_Pan	
Size A3	Project Name IAXBT-BL	Rev R1.01	
Date: Tuesday, February 11, 2014		Sheet 13	of 67

Berlin USB



<Verban Name> REGATRON DT-MB RESTRICTED SECRET

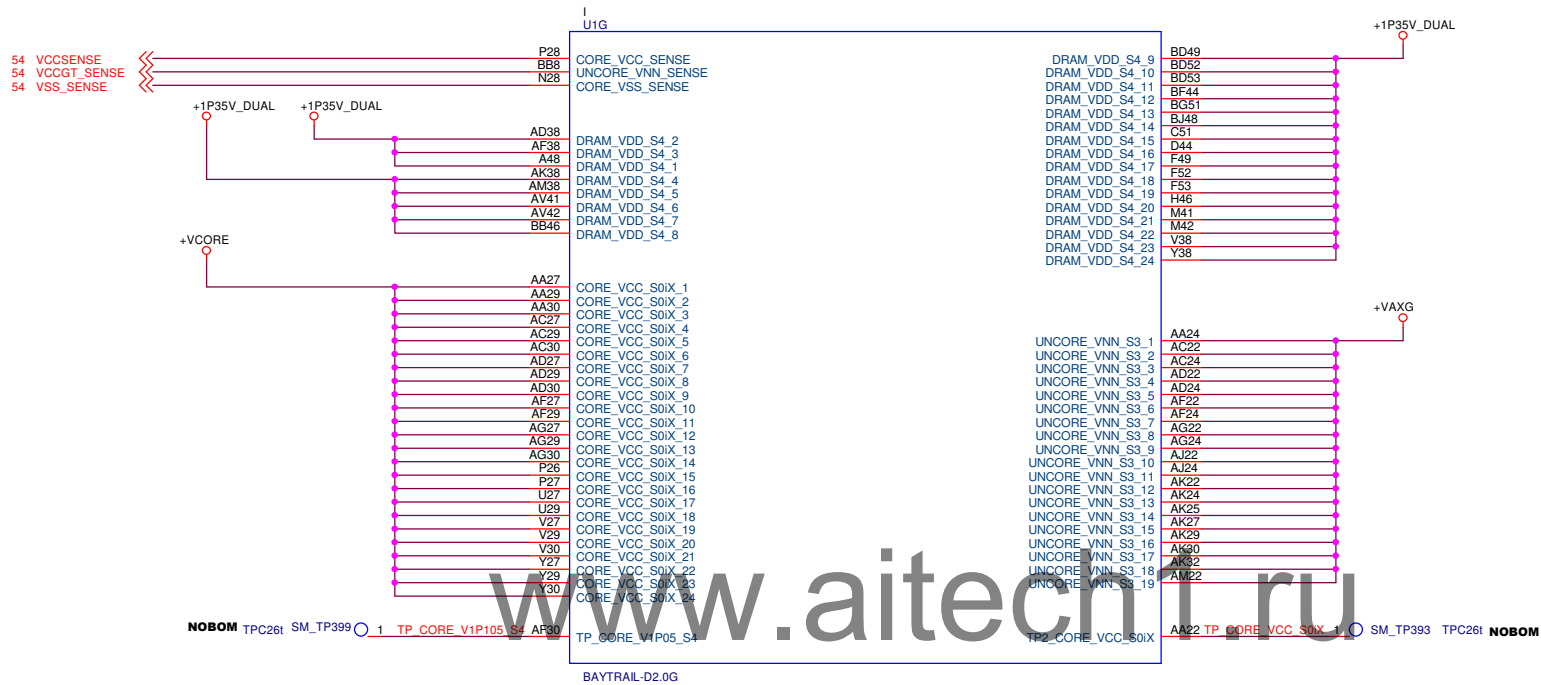
PEGATRON Title : SoC-6 USB

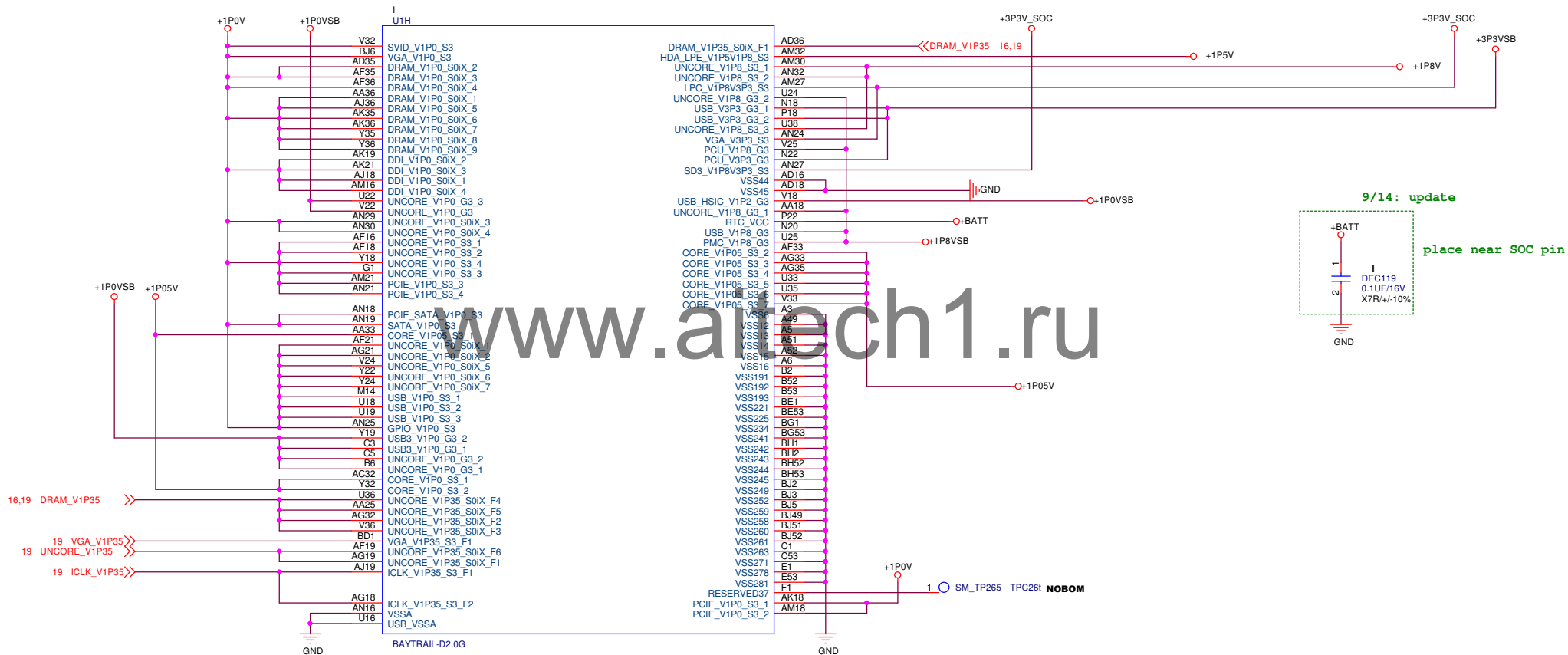
Pegatron Corp. Engineer: Wade_Pan

Size	Project Name	Rev
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A3	IAXBT-BL	R1.01
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Date: Tuesday, February 11, 2014 Sheet 14 of 67





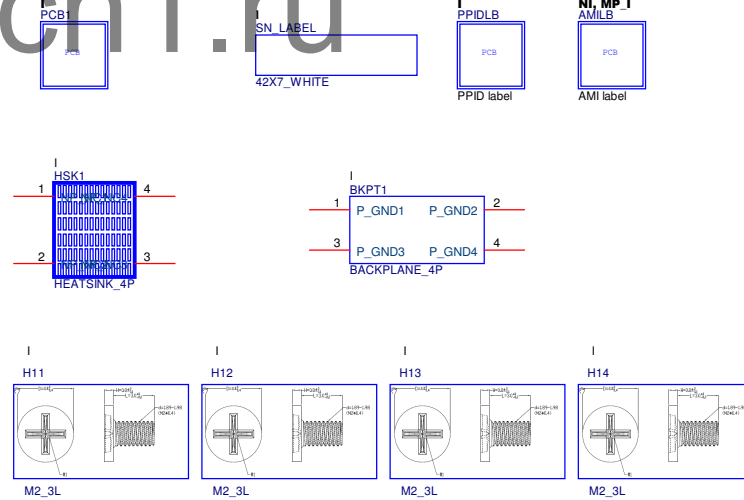
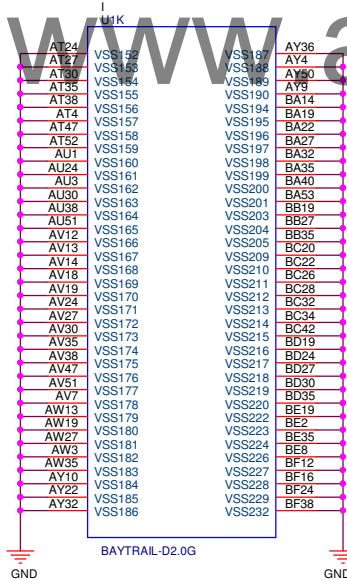
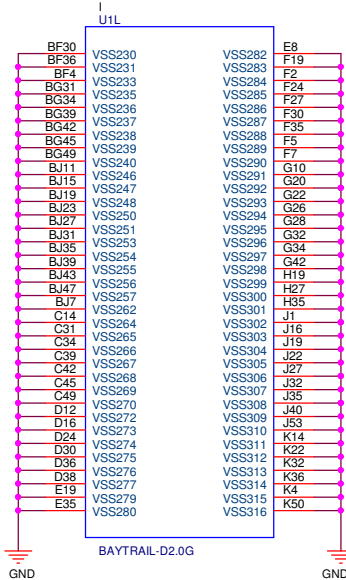
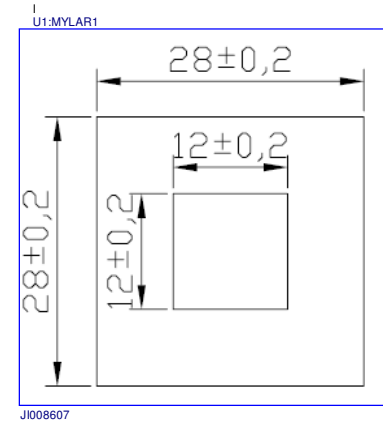
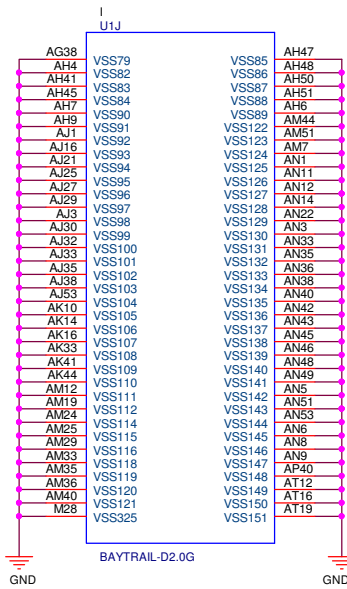
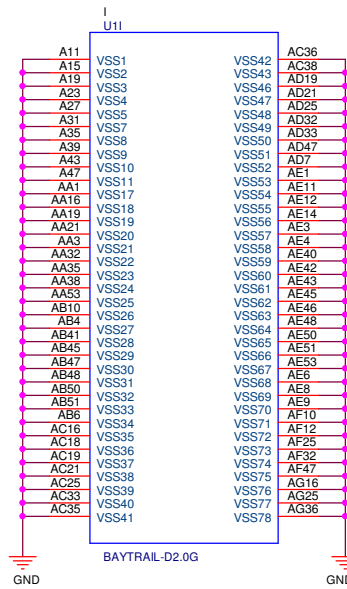
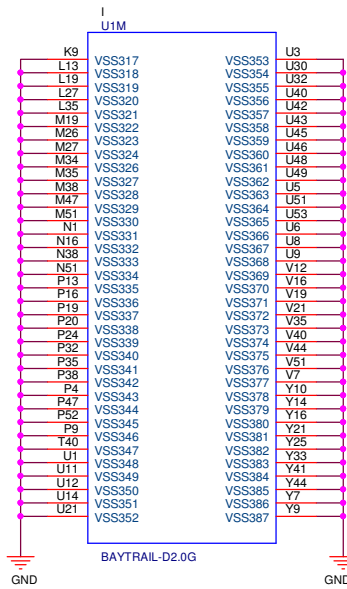
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SoC-8 POWER2

Pegatron Corp. Engineer: Wade_Pan

Size	Project Name	Rev
A3	IAXBT-BL	R1.01

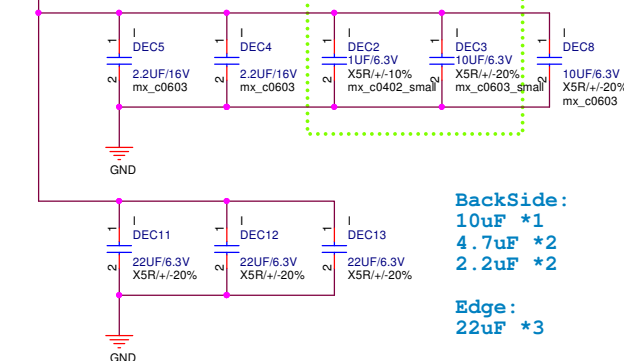
Date: Tuesday, February 11, 2014	Sheet 16 of 67
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22UF ALL USED 0805

10/24:
DEC2 from (4.7uF/6.3V/0402) to (1uF/6.3V/0402/small)
DEC3 from (4.7uF/6.3V/0402) to (10uF/6.3V/0603/small)

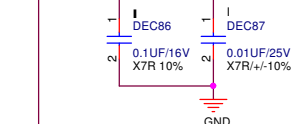
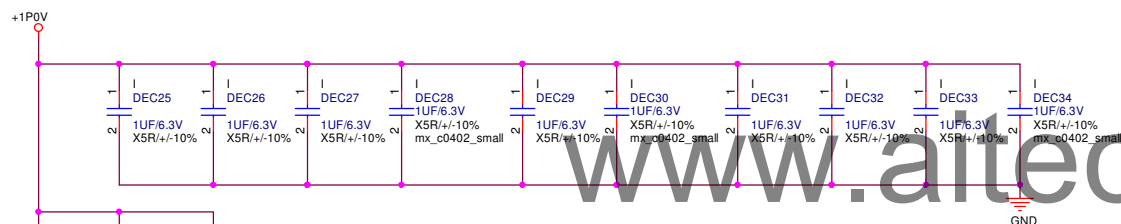
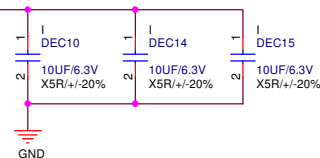


+VAXG

BackSide:
1uF *3

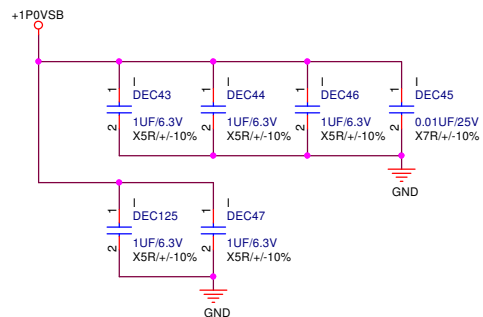
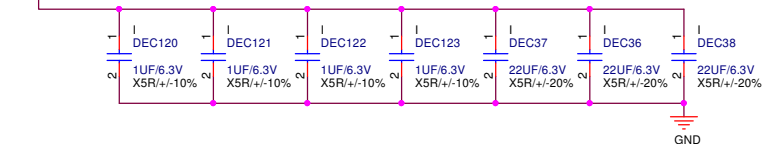
Edge:
10uF *3

(12/2)
DEL DEC1,6,7; DEC10, 14, 15 change to small



BackSide:
1uF *10
0.1uF *1
0.01uF *1

Edge:
1uF *4
22uF *3



BackSide:
1uF *3
0.01uF *1

Edge:
1uF *2

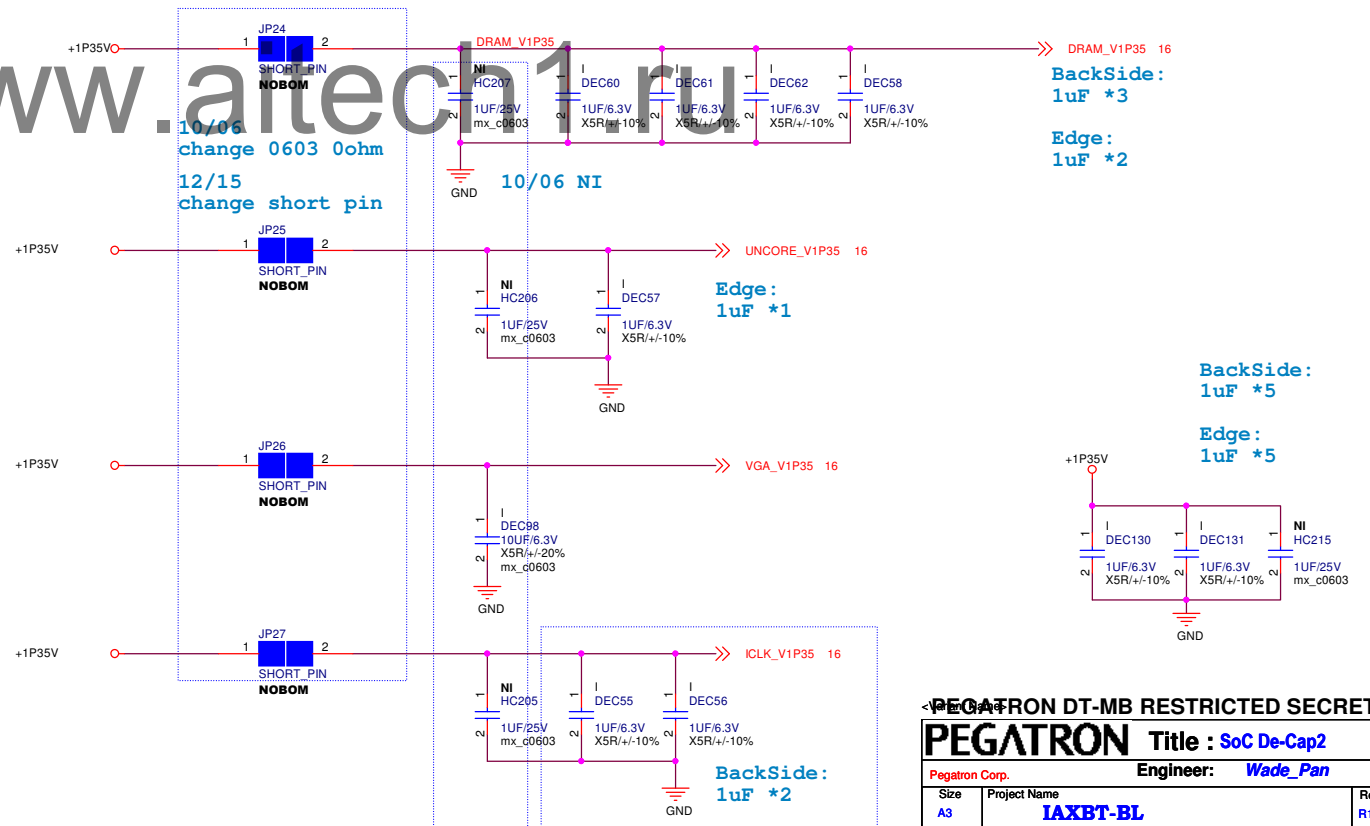
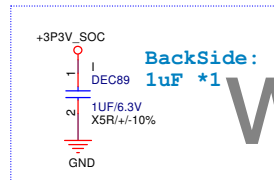
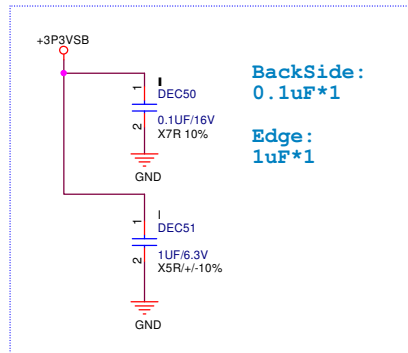
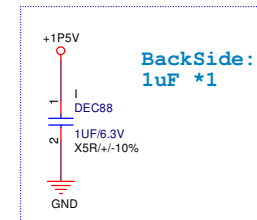
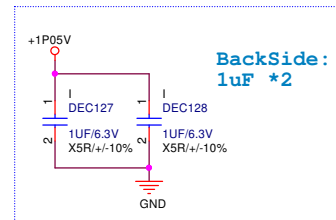
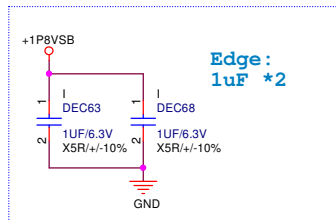
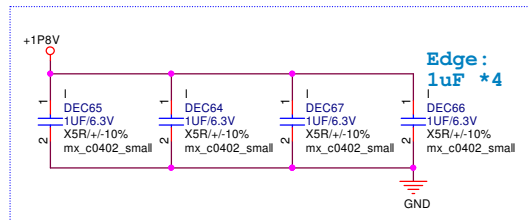
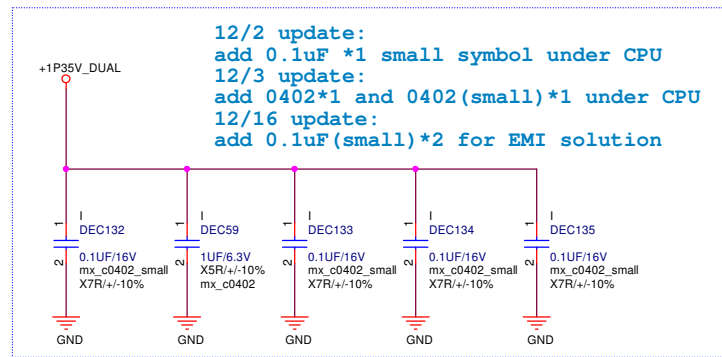
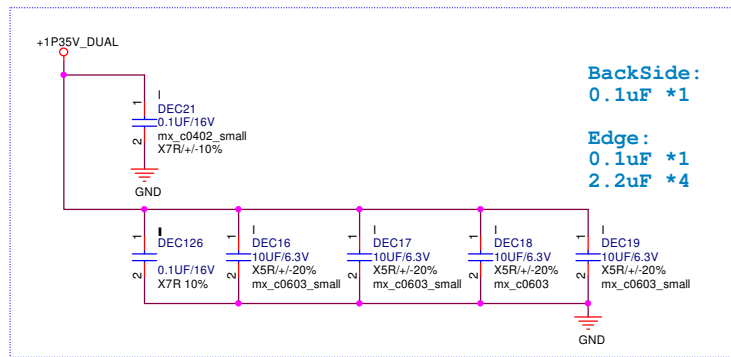
PEGATRON DT-MB RESTRICTED SECRET

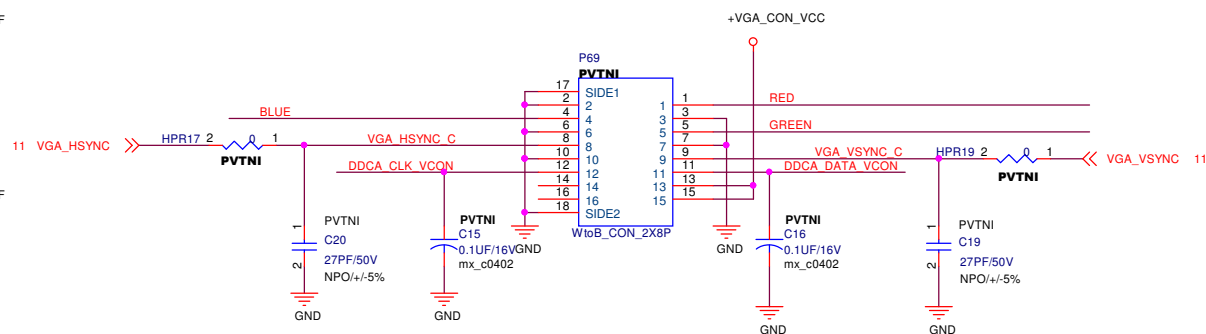
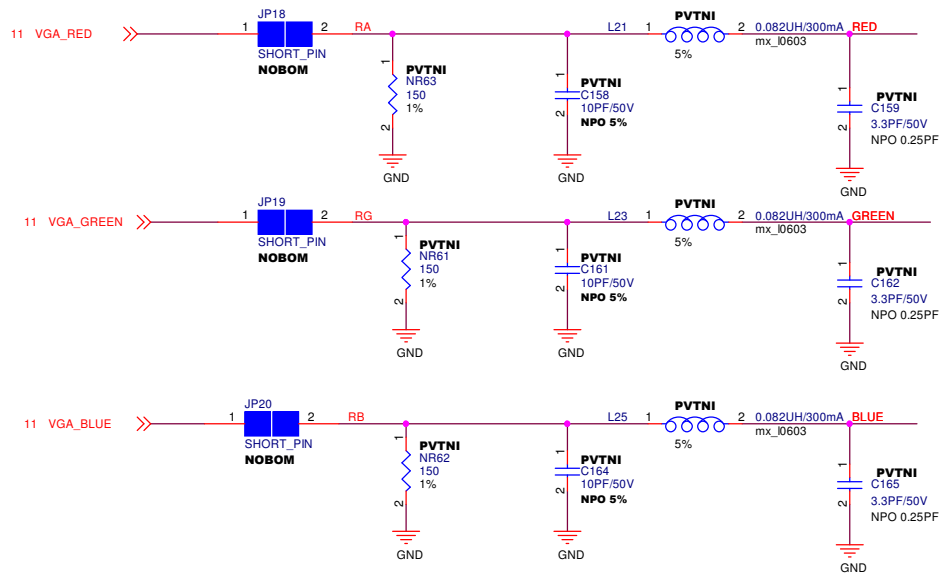
PEGATRON Title : SoC De-Cap1

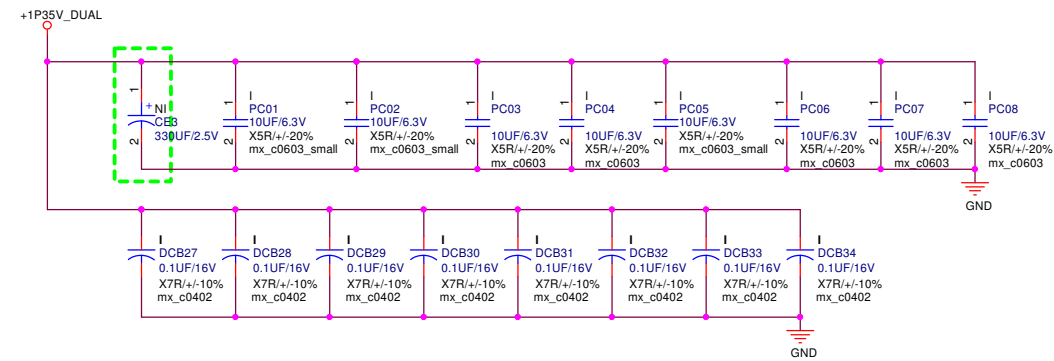
Pegatron Corp. Engineer: Wade_Pan

Size	Project Name	Rev
A3	IAXBT-BL	R1.01

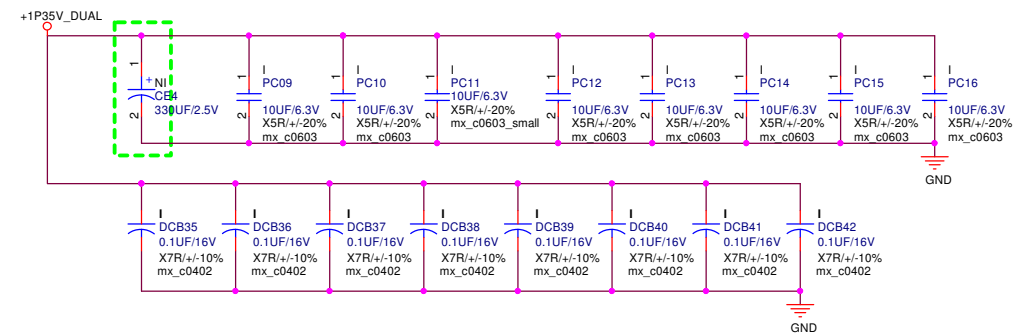
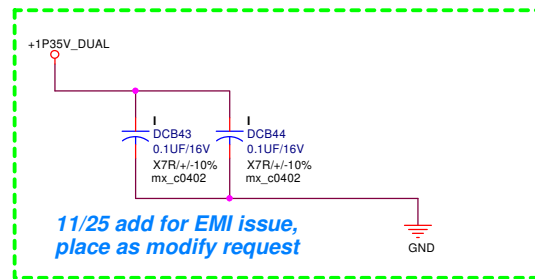
Date: Tuesday, February 11, 2014	Sheet 18 of 67
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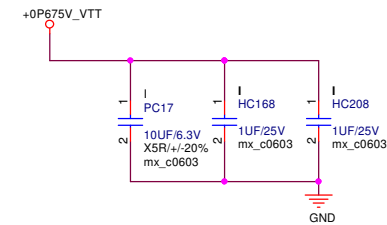


10/2, close to dimm0
330uF, 10uF(0603)

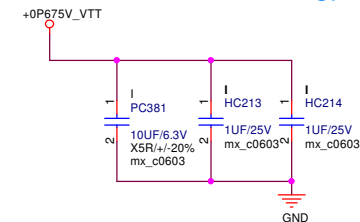


10/2, close to dimm1
330uF, 10uF(0603)

10/4, close to dimm0

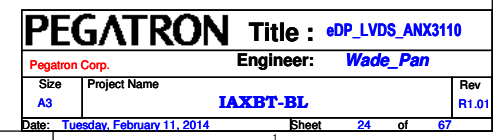


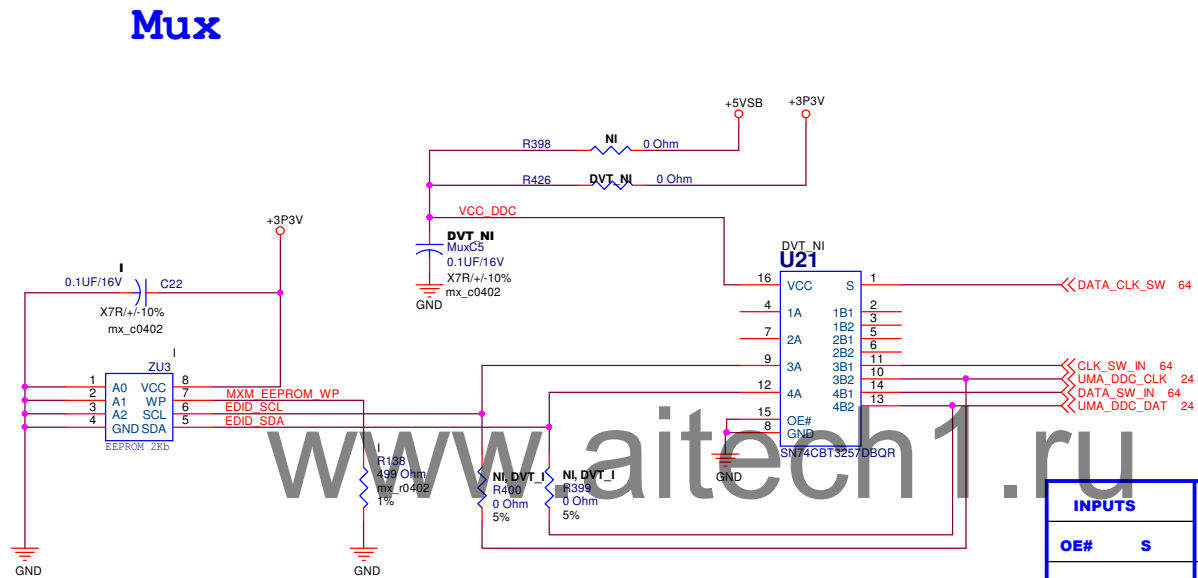
10/4, close to dimm1



PEGATRON DT-MB RESTRICTED SECRET

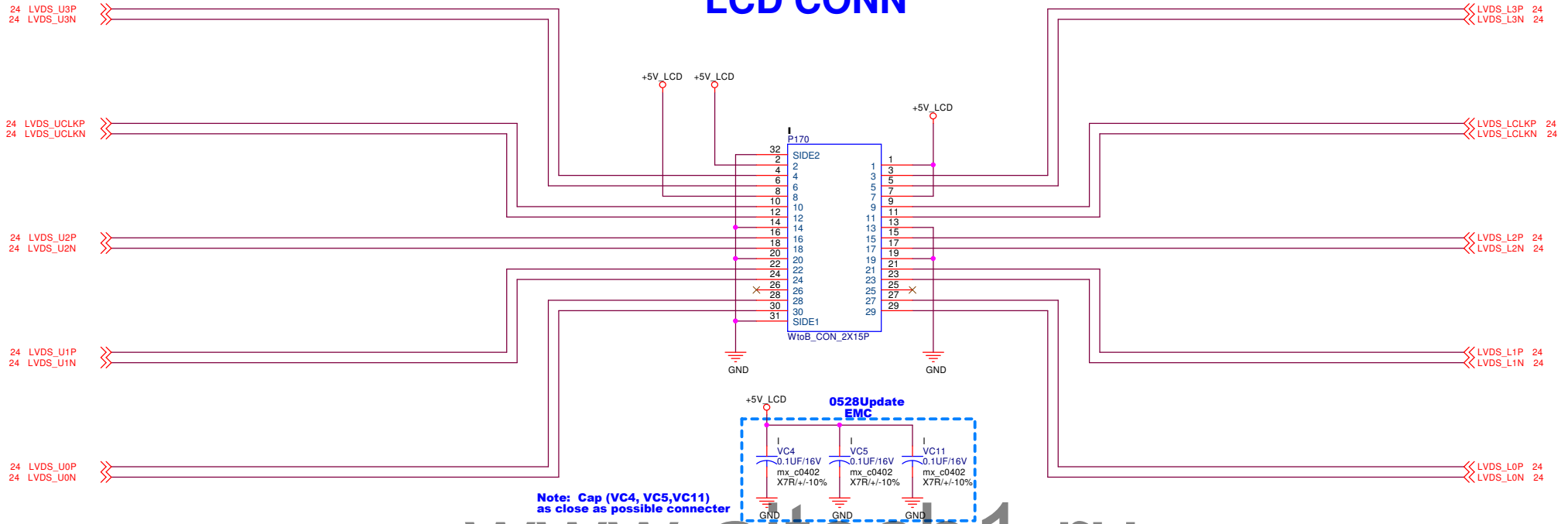
PEGATRON		Title :DDR3 TERMINATION A&B	
Pegatron Corp.		Engineer: Wade_Pan	
Size A3	Project Name IAXBT-BL	Rev R1.01	
Date: Tuesday, February 11, 2014		Sheet 23 of 67	





INPUTS		FUNCTION
OE#	S	
L	L	A Port=B1 Port
L	H	A Port=B2 Port
H	X	Disconnect

LCD CONN



LCD ON/OFF

0523 Update

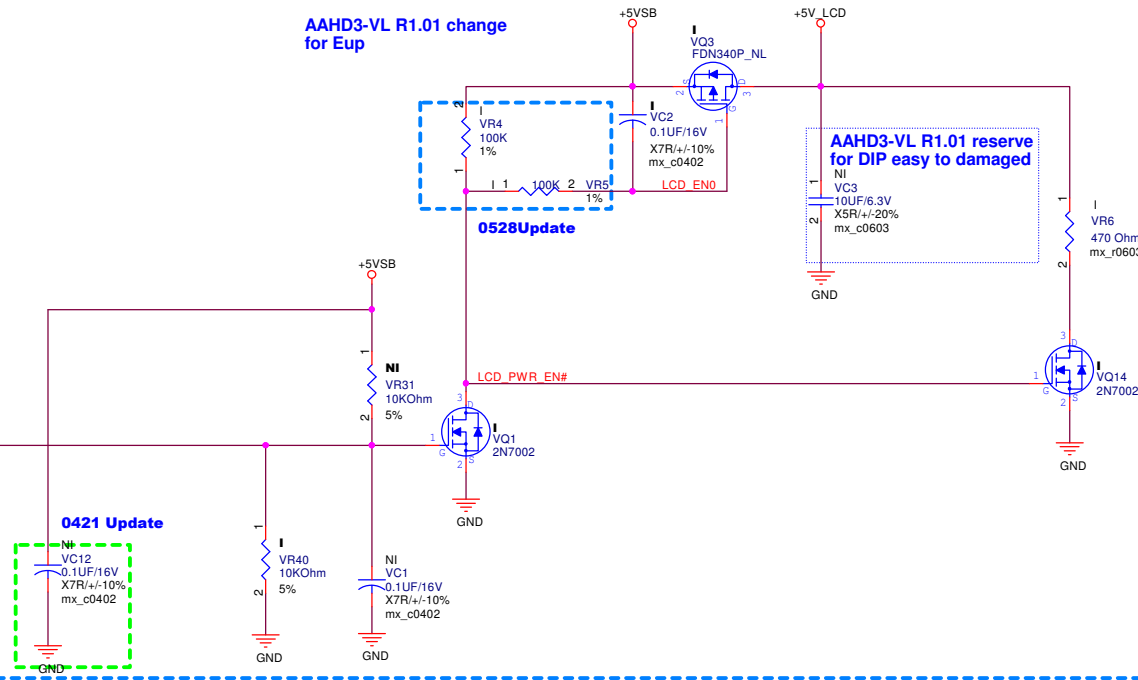
AAHD3-VL R1.01 change for Eup

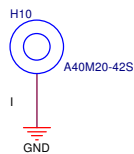
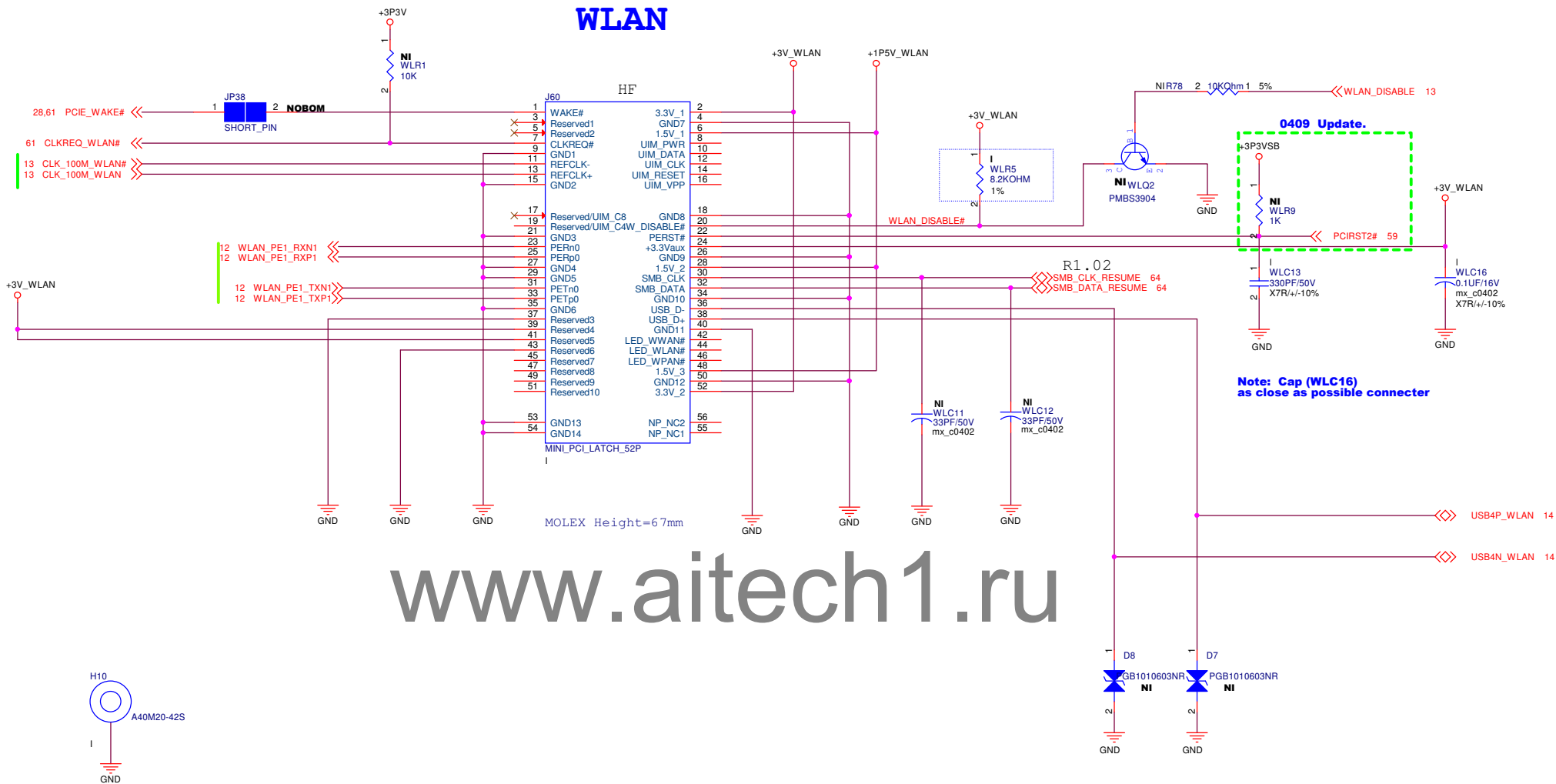
0401 Update

0421 Update

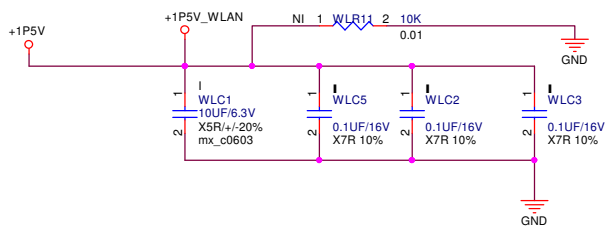
0528Update

AAHD3-VL R1.01 reserve for DIP easy to damaged

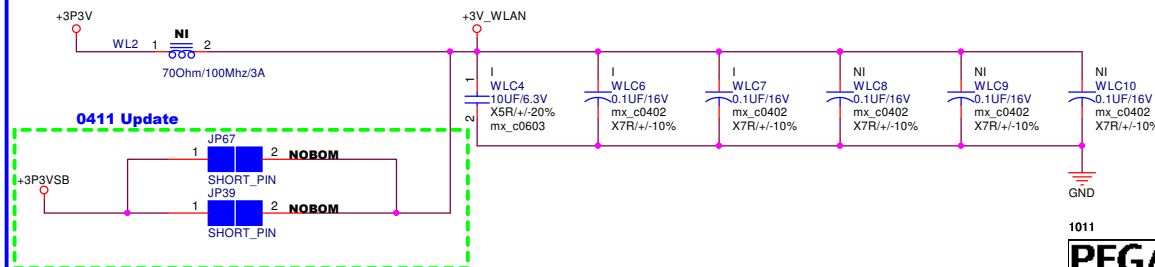




+1P5V_WLAN

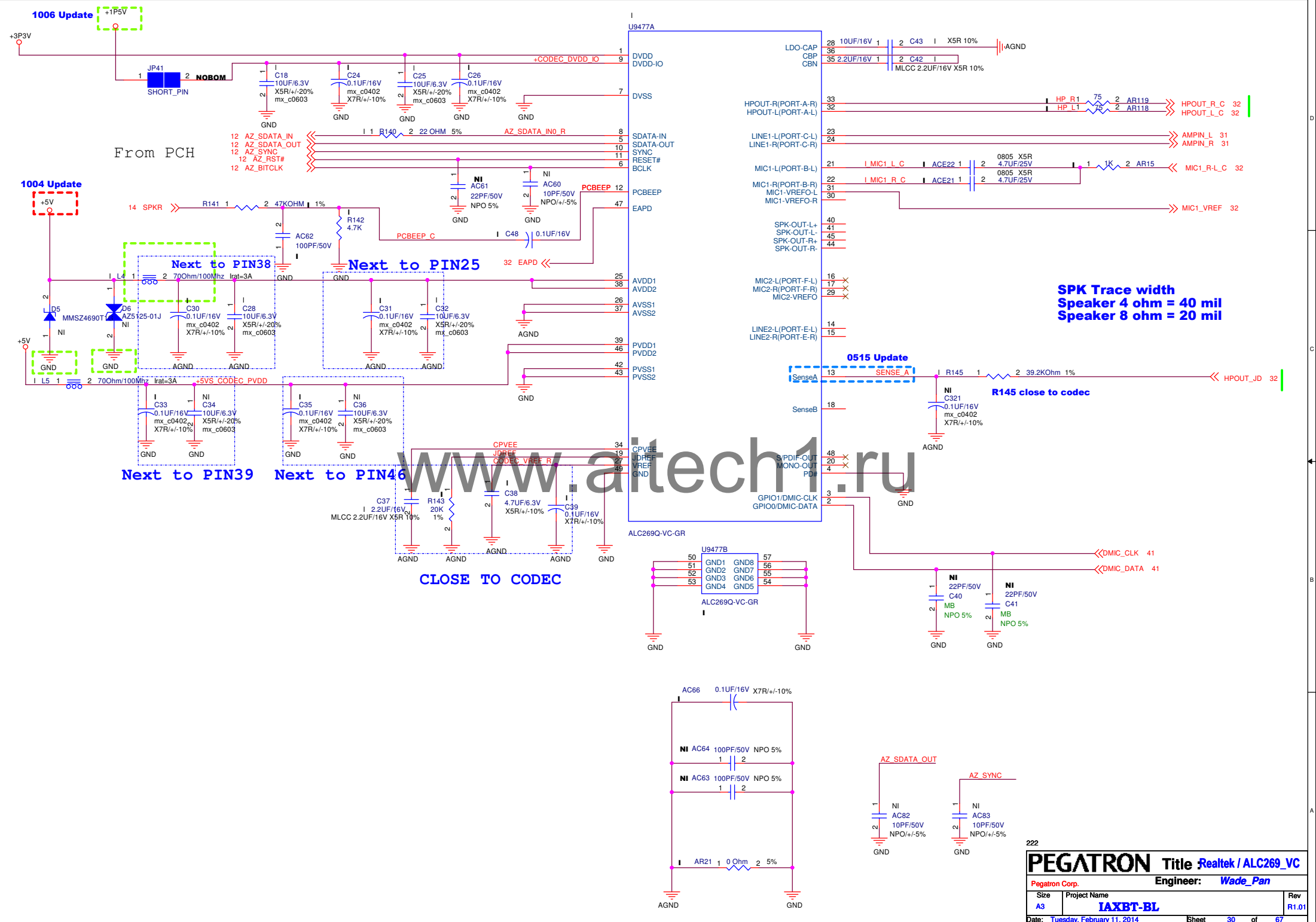


+3V_WLAN

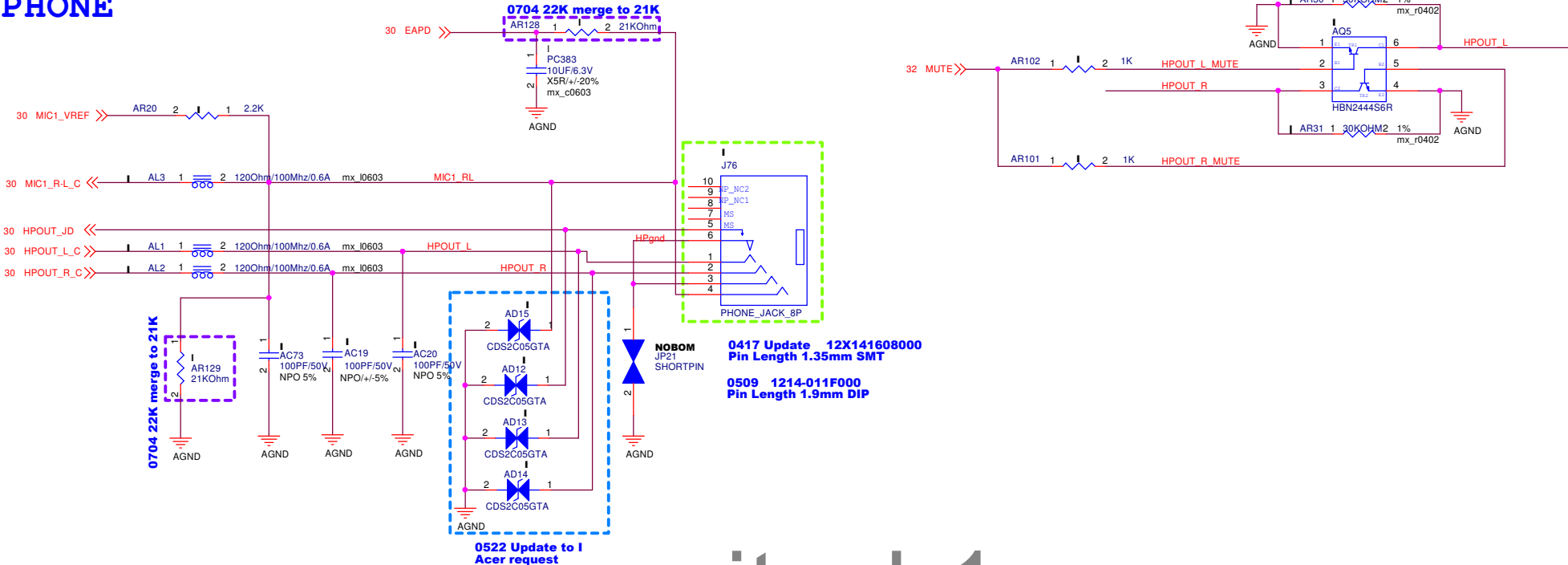


1011

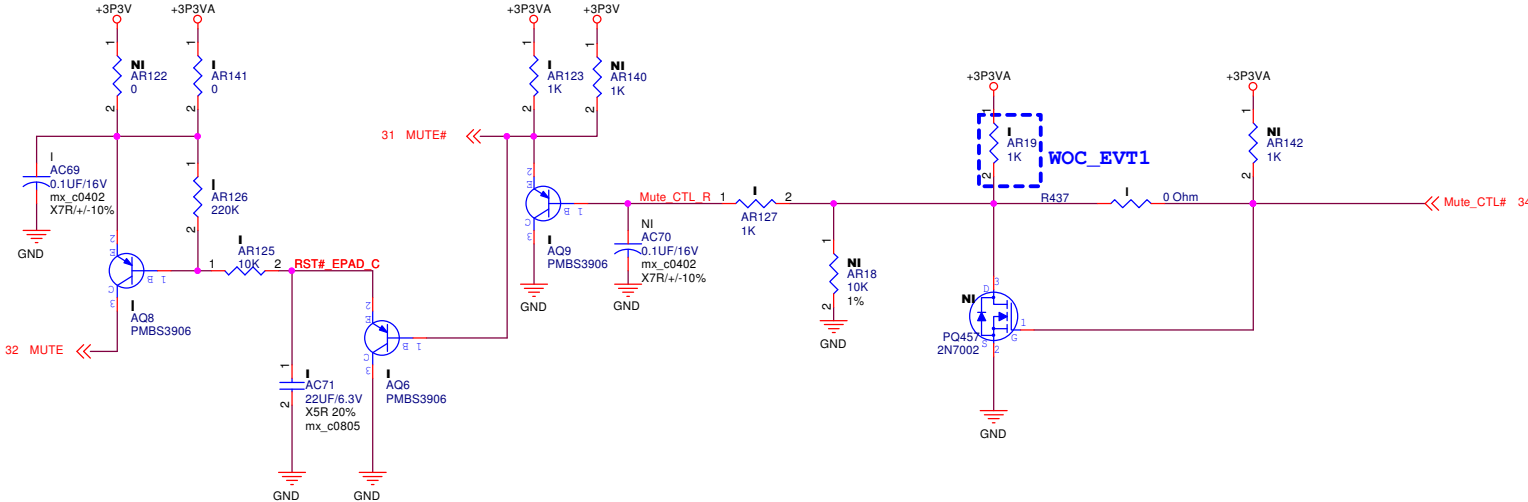
PEGATRON		Title : MINI Card WLAN	
Pegatron Corp.		Engineer: Wade_Pan	
Size A3	Project Name IAXBT-BL		Rev R1.01
Date: Tuesday, February 11, 2014		Sheet 27 of 67	



HEADPHONE

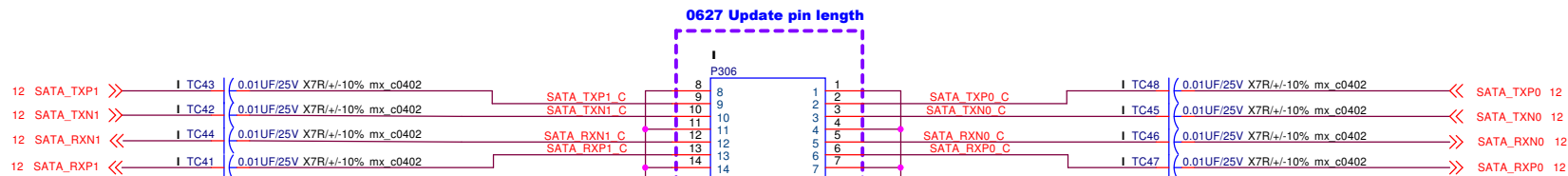


Audio MUTE



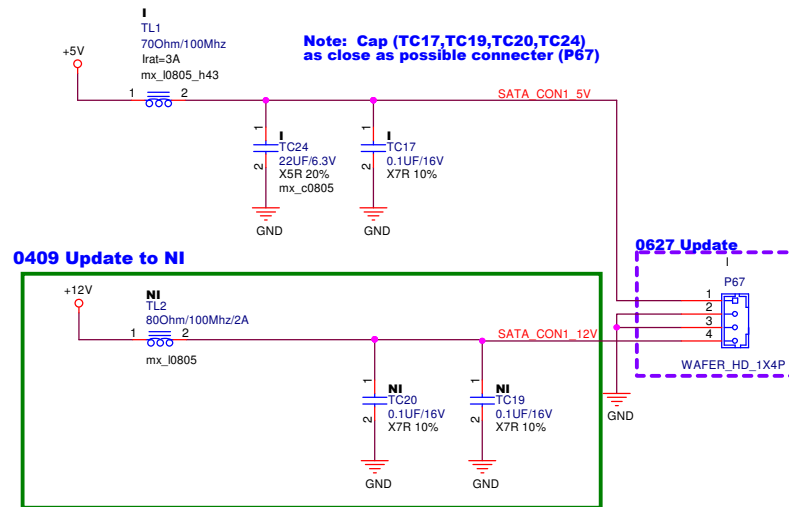
LAYOUT NOTE:
 Two Strobes : Matched within 100 mils of each other
 D[0:15] : Matched within +/- 450 mils of two strobes

SATA CONNECTOR

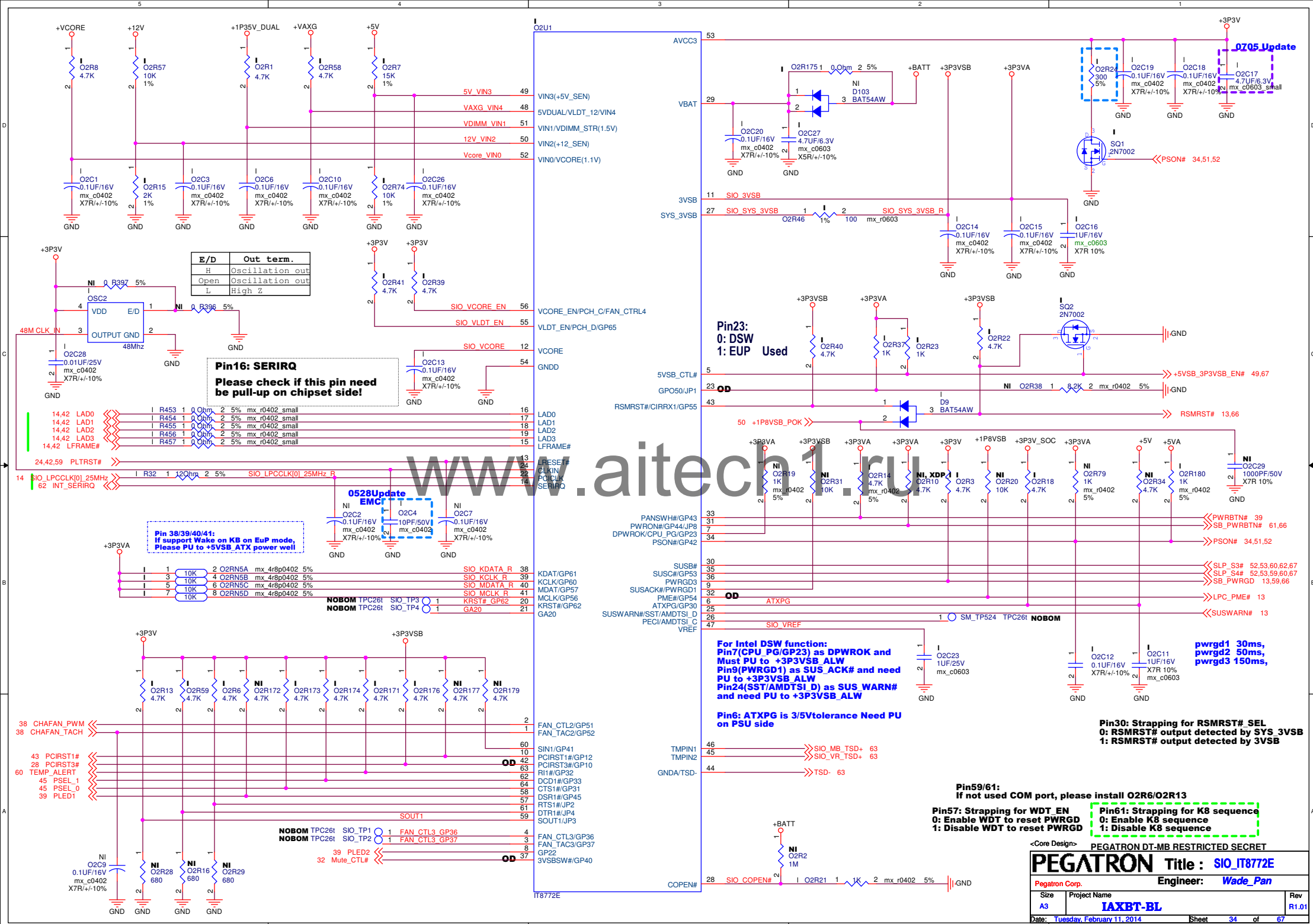


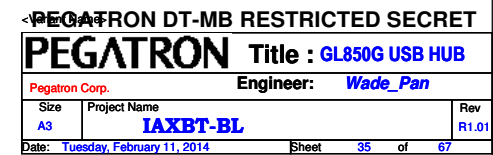
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Note: Cap (TC17,TC19,TC20,TC24) as close as possible connector (P67)



222



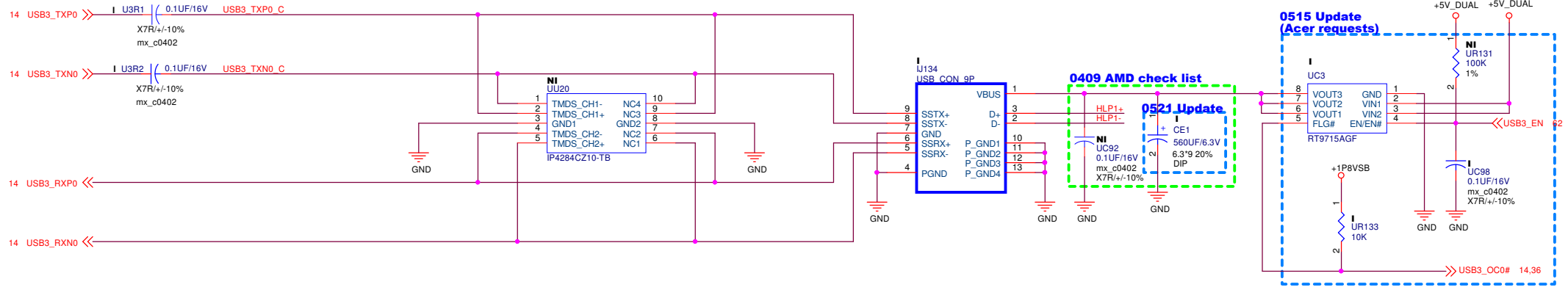


SIDE USB3.0

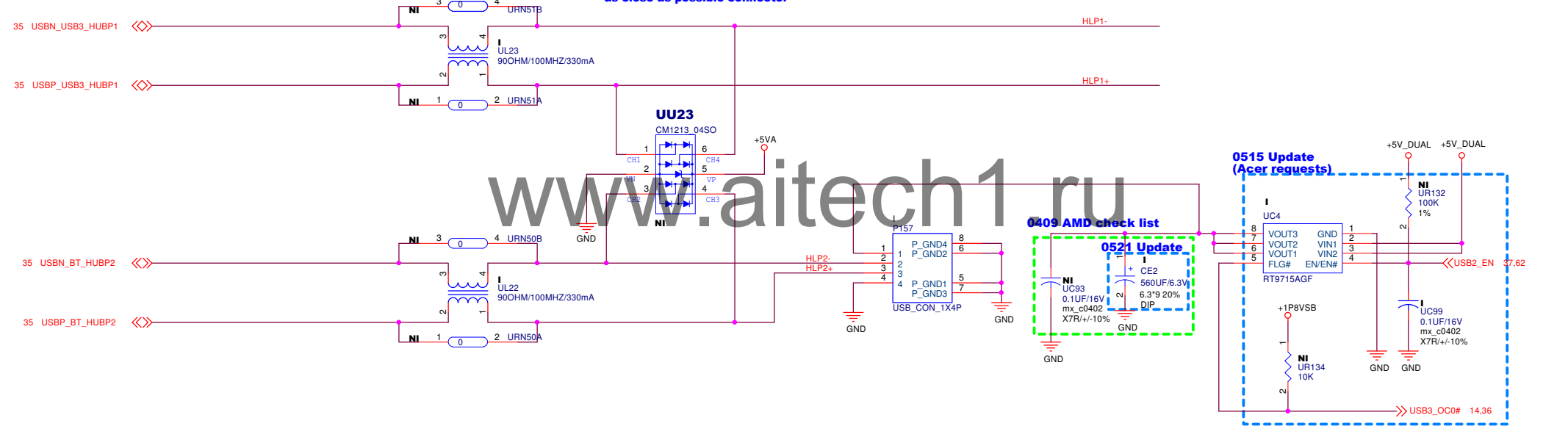
NOTE:

0722-0066000 ESD PROTECTION SOT1059 NXP/IP4284CZ10-TB

0722-003Y000 ESD PROTECTION TSLP-9-1 INFINEON/ESD5V3U4U-HDMI



Note: ESD (UU21) and Cap (UCE1,UCE2,UC92,UC93) as close as possible connector



1213-00LN000 USB2.0

PIN NO.	1	2	3	4
SIGNAL NAME	VBUS	D-	D+	PGND
REMARK	USB2.0 CONTACT PIN			

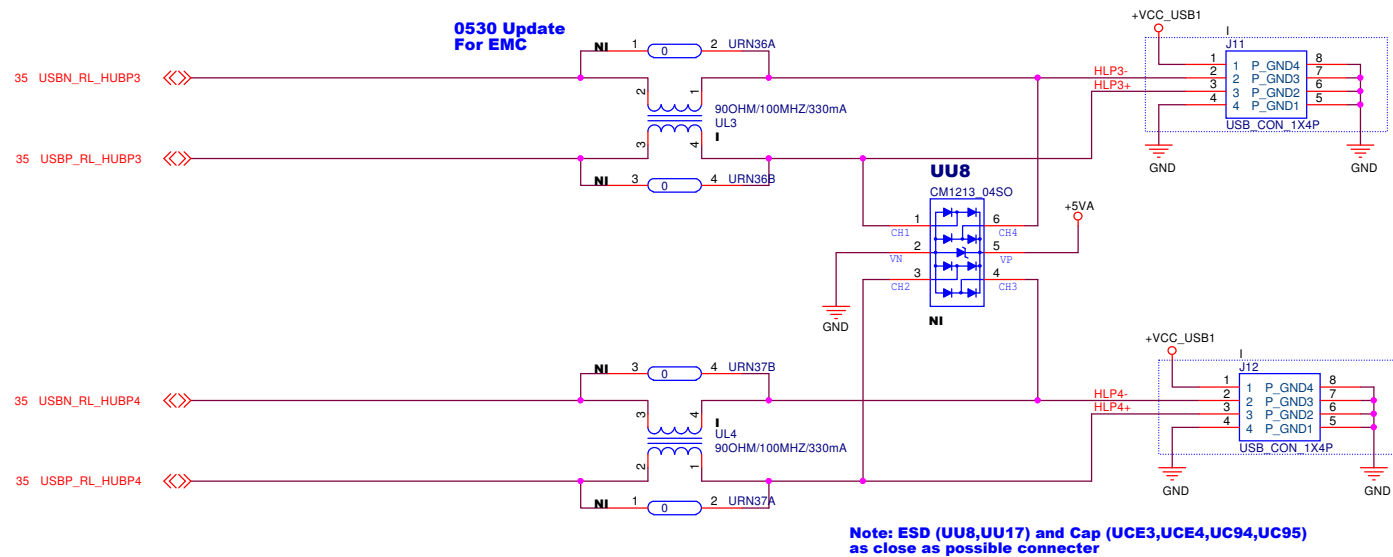
<Core Design>

PEGATRON Title : SIDE USB3.0/USB2.0 FOR

Pegatron Corp. Engineer: Wade_Pan

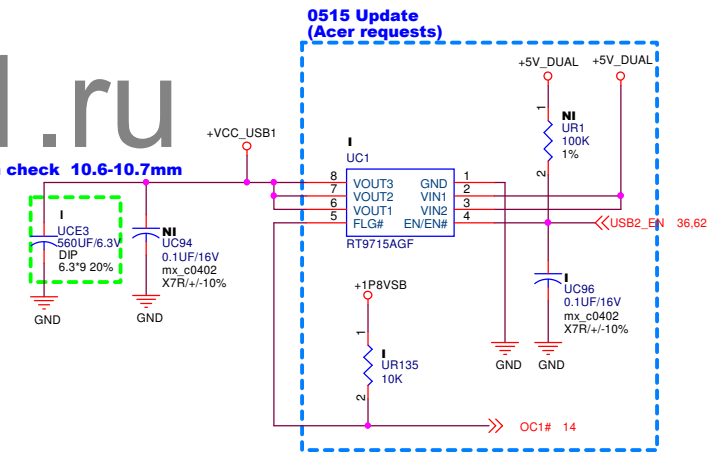
Size A3 Project Name IAXBT-BL Rev R1.01

Date: Tuesday, February 11, 2014 Sheet 36 of 67



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0409 Z-high check 10.6-10.7mm

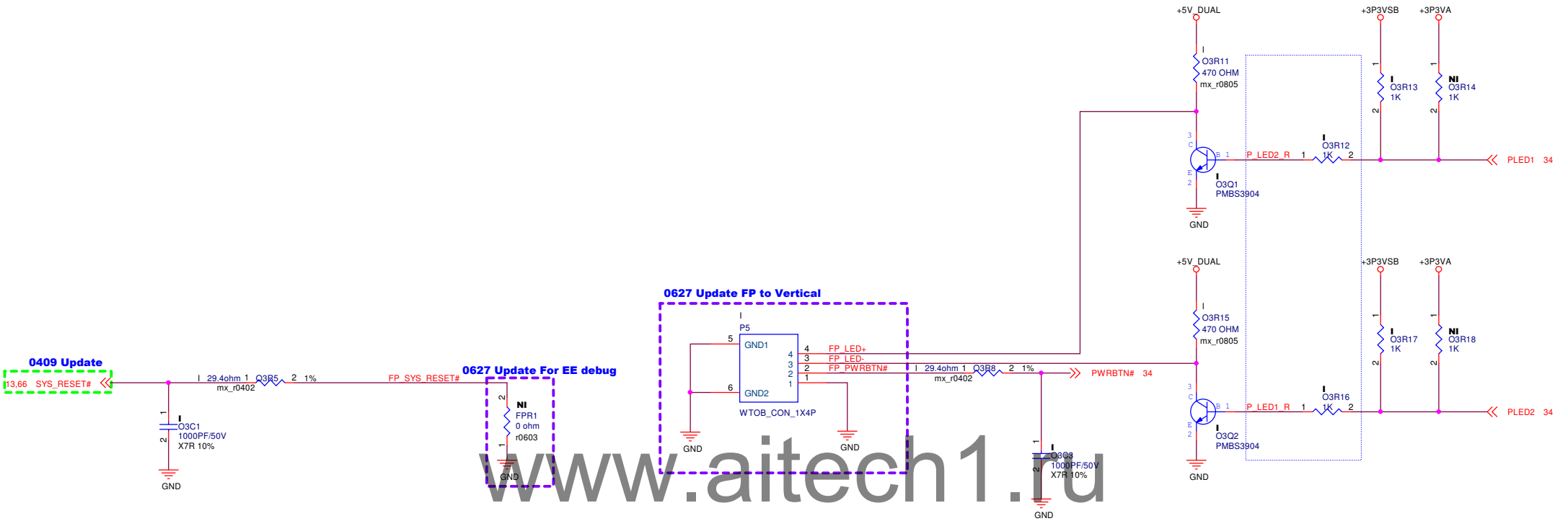


R1.02---2010/05/18:Exchange SYS FAN & CPU FAN Connector.



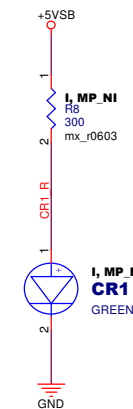
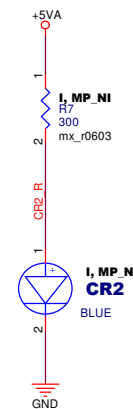
FRONT PANEL / LED CIRCUITRY

AAHD3-AG 1.01 Change
for Erp



+5VA : BLUE

+5VSB : GREEN



1011

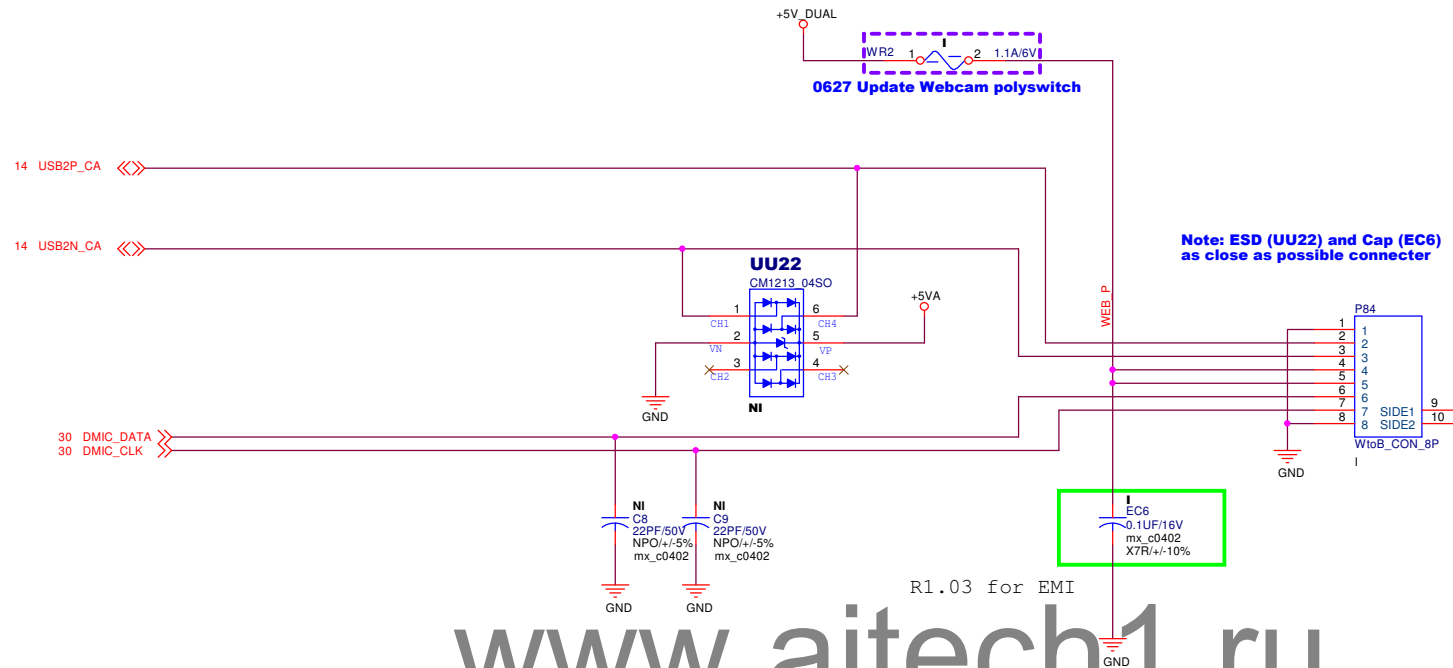
PEGATRON		Title : FR PANEL/LED	
Pegatron Corp.		Engineer: <i>Wade_Pan</i>	
Size A3	Project Name IAXBT-BL	Rev R1.01	
Date: Tuesday, February 11, 2014		Sheet	39 of 67

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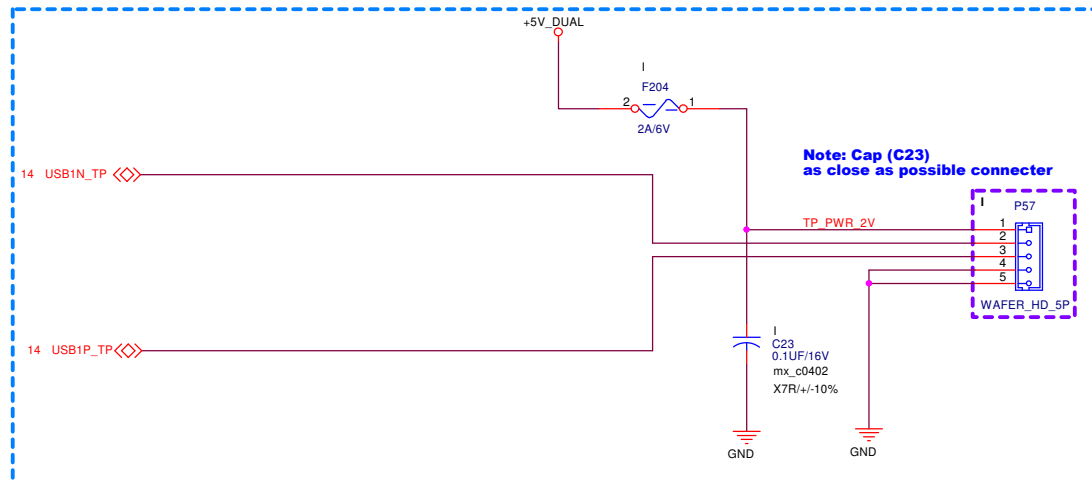
1011

PEGATRON		Title : <i>reserve</i>	
<i>Pegatron Corp.</i>		Engineer: <i>Wade_Pan</i>	
Size	Project Name		Rev
A3	IAXBT-BL		R1.01
Date: <i>Tuesday, February 11, 2014</i>		Sheet	40 of 67

Webcam & Digital MIC CONNECTOR



Touch Panel



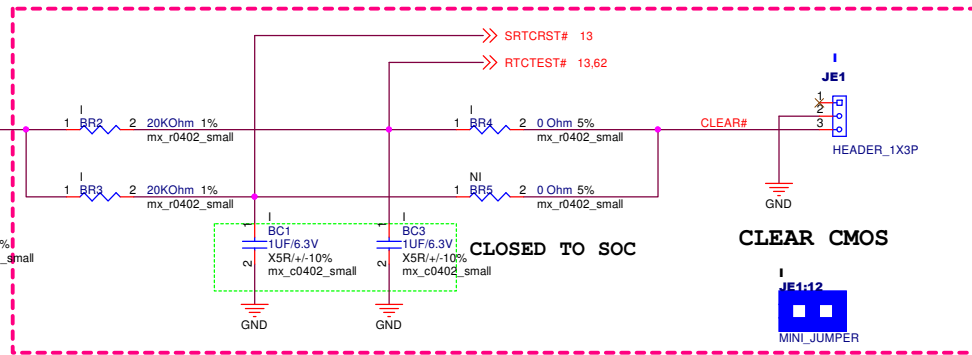
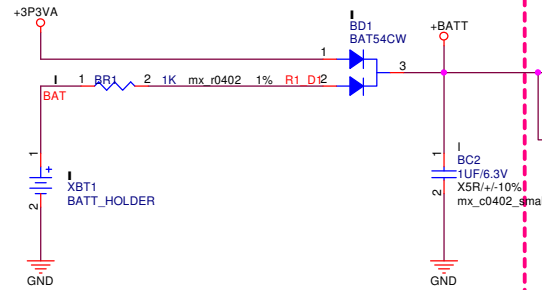
1011

PEGATRON			Title :WEB CONN&TOUCH CONN	
Pegatron Corp.			Engineer: Wade_Pan	
Size	Project Name			Rev
A3	IAXBT-BL			R1.01
Date: Tuesday, February 11, 2014		Sheet 41 of 67		

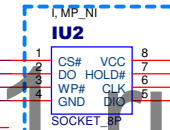
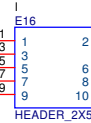
External RTC Circuitry

SRTCST#: resets all register bits in the RTC well
RTCTEST#: clear the RTC CMOS RAM.

Battery Socket



VCC=1.65~1.95
BIOS FLASH

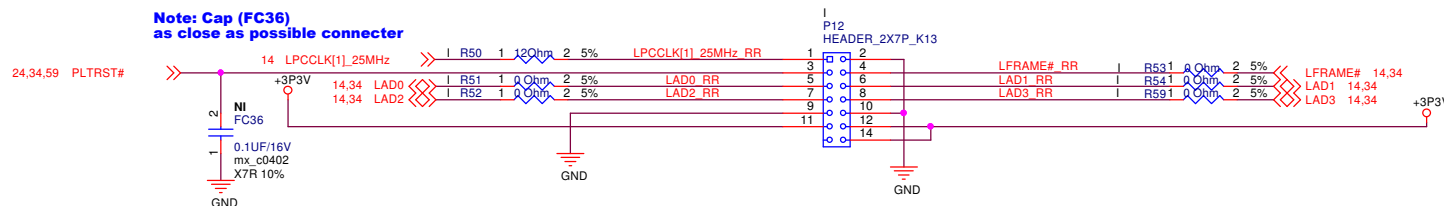


NOTE: New SPI ROM 8MB

IU1:
 NPI- DIP
 MP- SMD

LPC DEBUG

Note: Cap (FC36)
 as close as possible connector



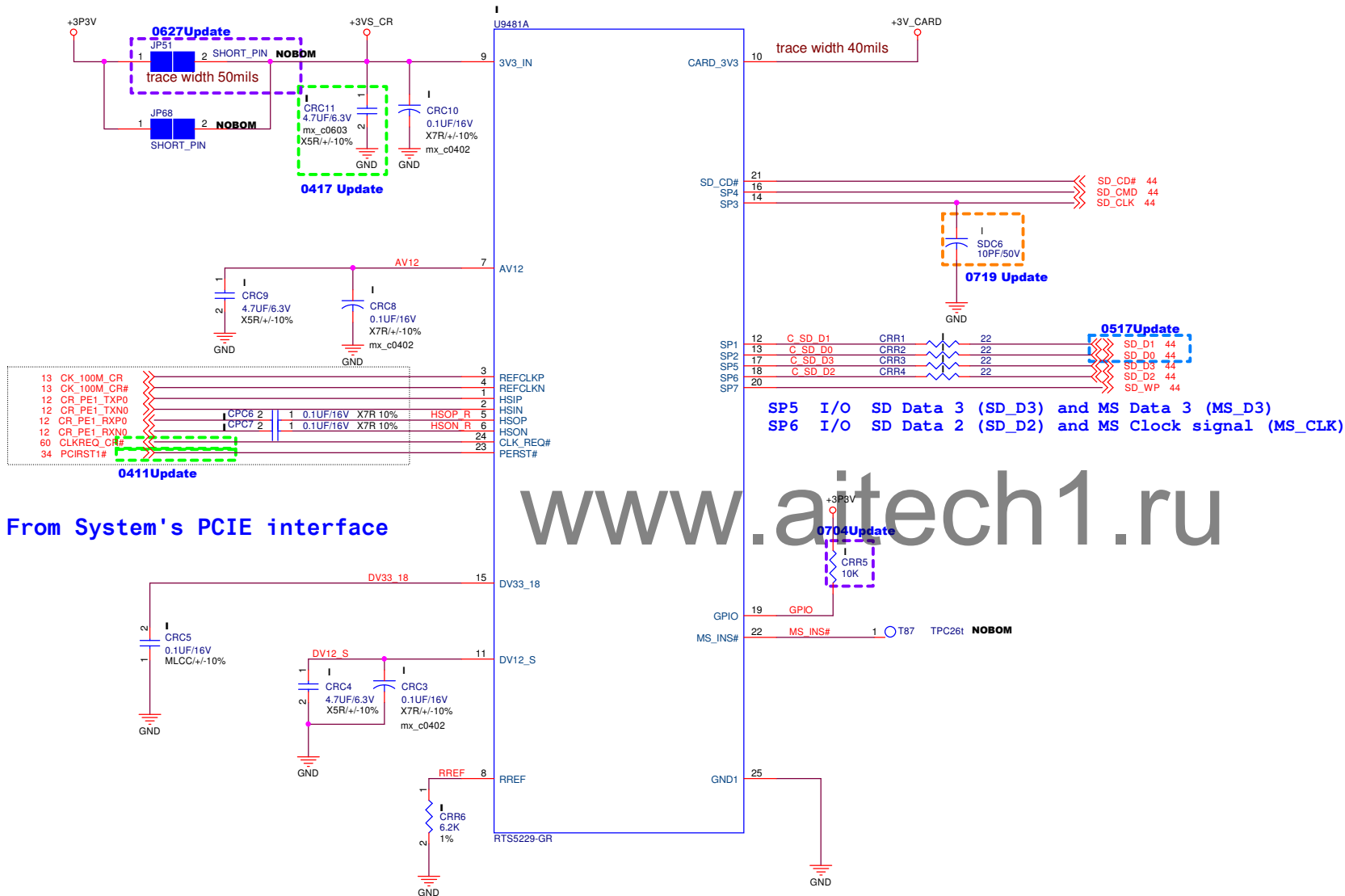
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **RTC/ SPI/ LPC DEBUG**

Engineer: **Wade_Pan**

Size **A3** Project Name **IAXBT-BL** Rev **R1.01**

Date: **Tuesday, February 11, 2014** Sheet **42** of **67**



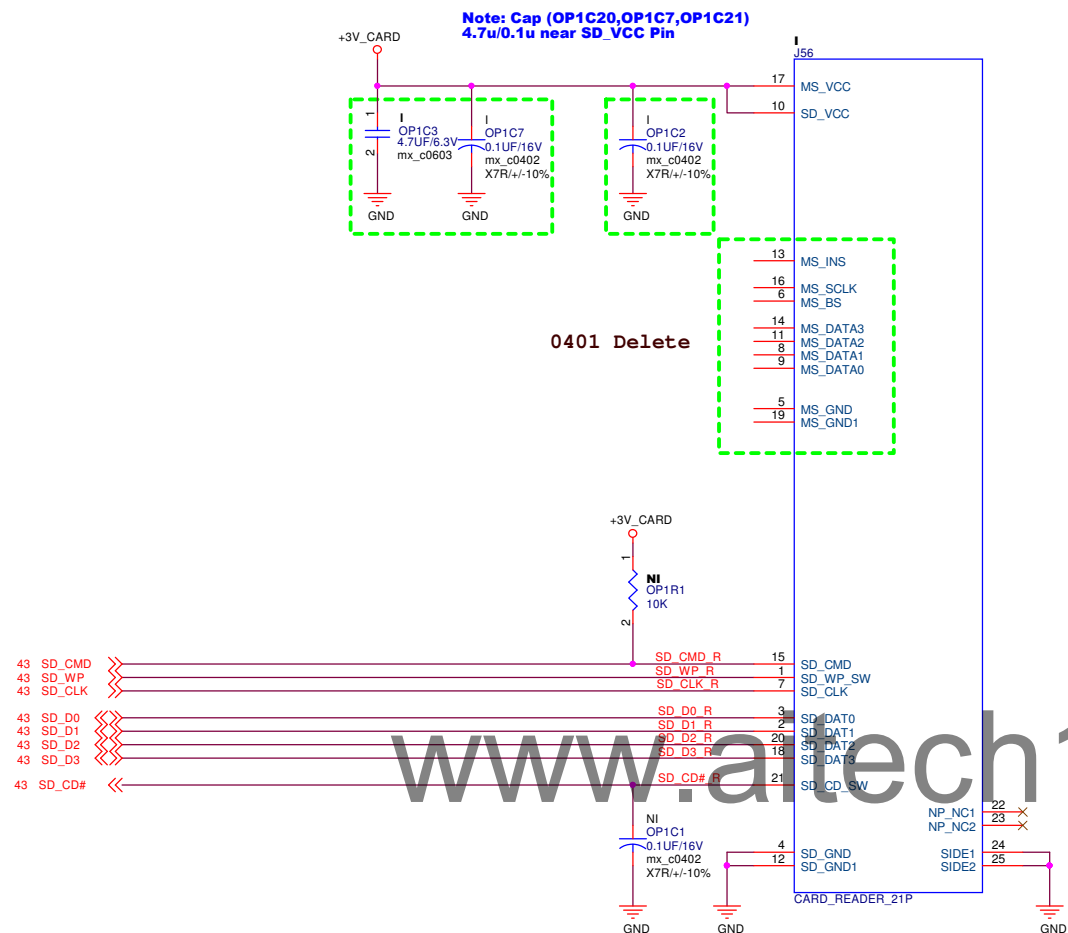
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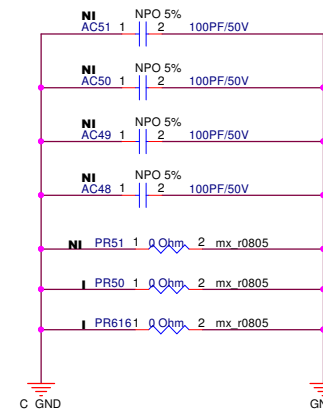
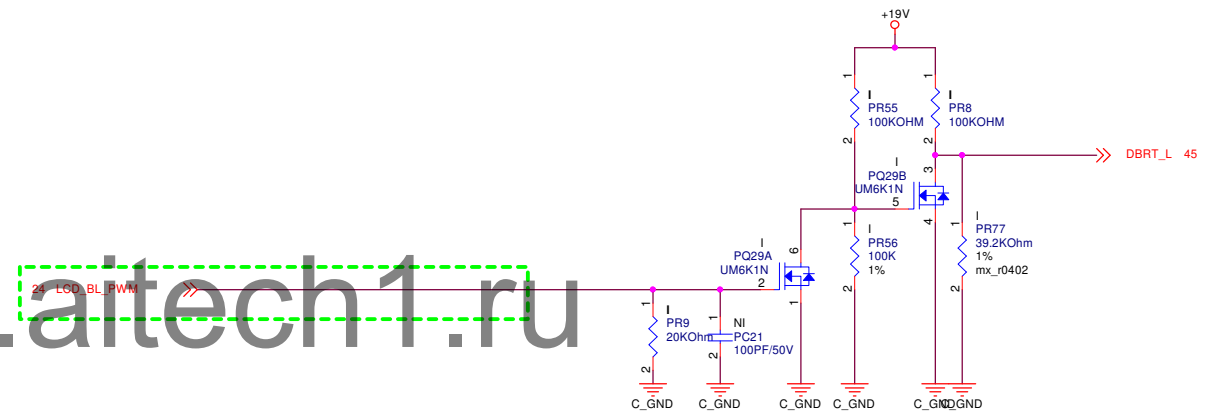
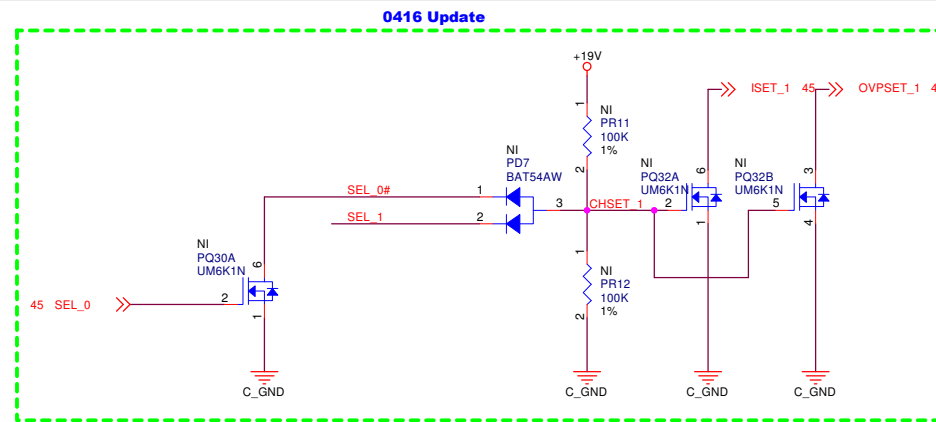
PEGATRON Title **CARREADER RTS5229**

Pegatron Corp. Engineer: **Wade_Pan**

Size	Project Name	Rev
A3	IAXBT-BL	R1.01

Date: **Tuesday, February 11, 2014** Sheet **43** of **67**



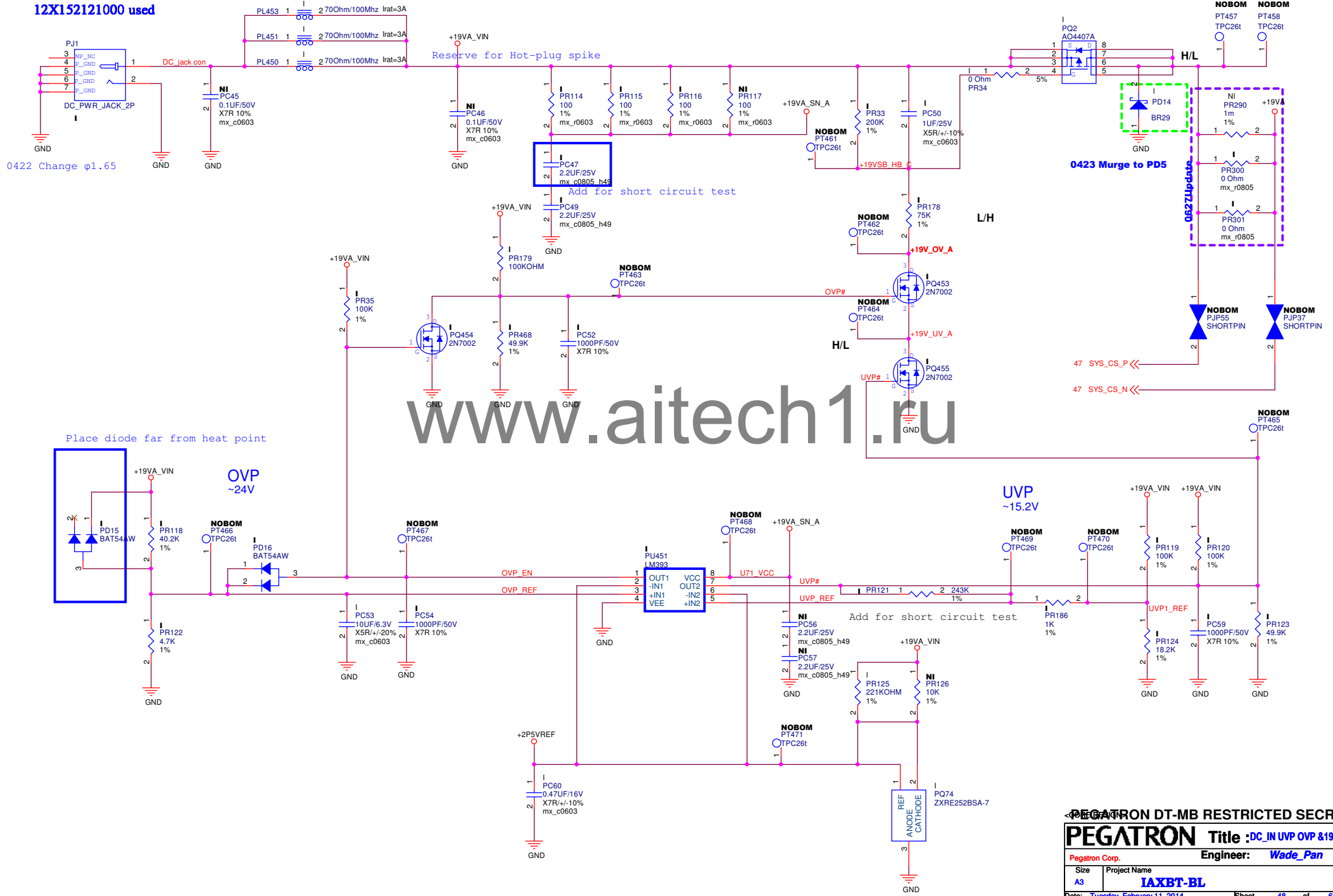


Adapter Input Connector

12X08705B080

12X08404B000

12X152121000 used



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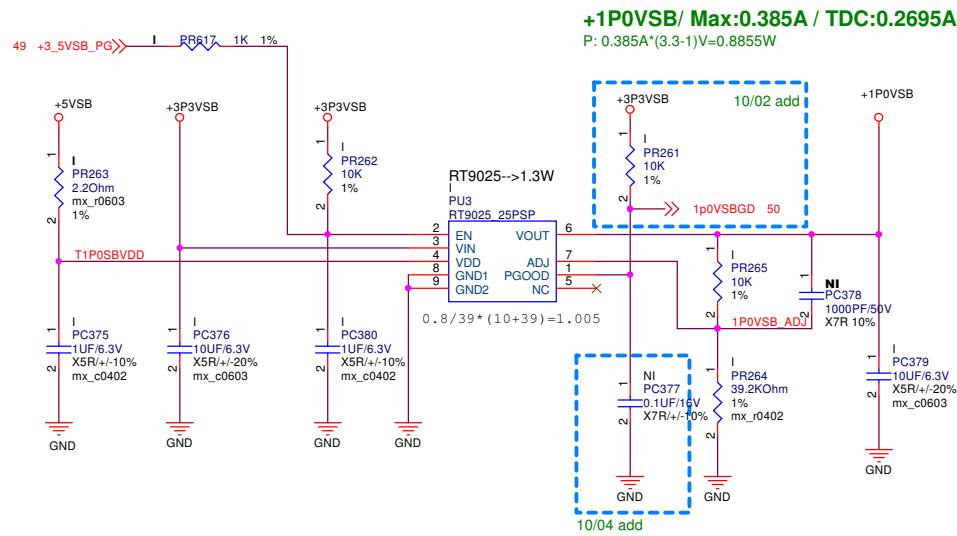
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title :DC_IN UVP OVP &19VSB

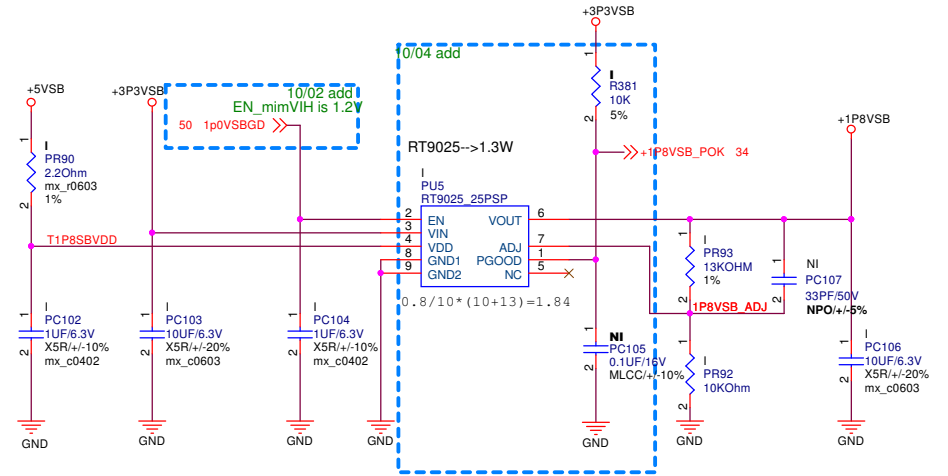
Pegatron Corp. Engineer: Wade_Pan

Size	Project Name	Rev
A3	IAXBT-BL	R1.01

Date: Tuesday, February 11, 2014 Sheet 48 of 67



+1P8VSB/ Max:0.084A / TDC:0.0588A
 $P: 0.084A \cdot (3.3-1.8)V = 0.126W$



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+12VA/ Max:0.736A / TDC: 0.5152A

Fsw = 500kHz
 lin= 0.581A
 Delta I =0.88A
 ripple =
 OCP = 5.5A

0416 Update

0510 Update

0627 Update

0522Update

0627Update

OCP=5.5A

$RILIM=[ILIMIT*24.14*(1+0.024*(ILIMIT-3.5))-1.8]$

$0.8/3.32*(47+3.32)=12.125$

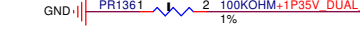
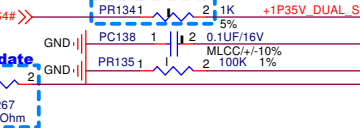
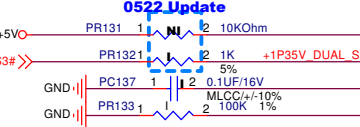
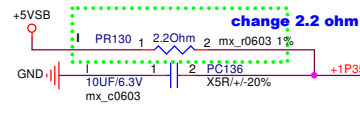
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : 12V

Pegatron Corp. Engineer: Wade_Pan

Size A3	Project Name IAXB-T-BL	Rev R1.01
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Date: Tuesday, February 11, 2014 Sheet 51 of 67



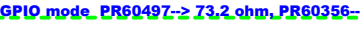
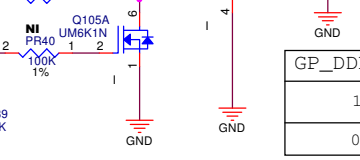
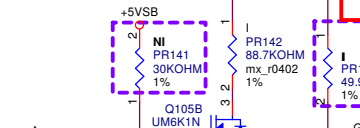
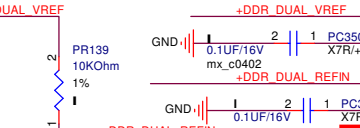
1122 Update

$$I_{ocp} = (V_{trip}/R_{DSon}) + (I_{ripple}/2)$$

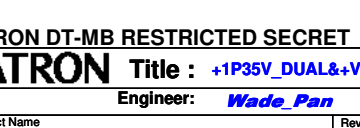
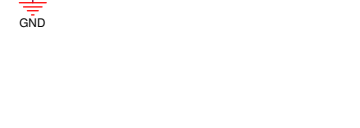
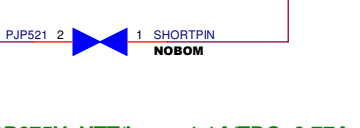
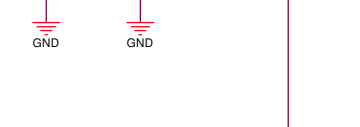
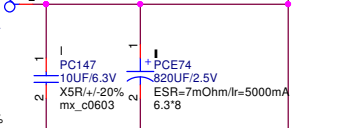
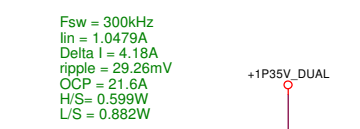
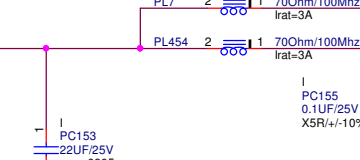
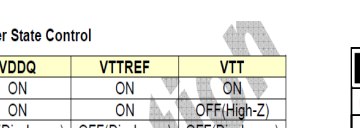
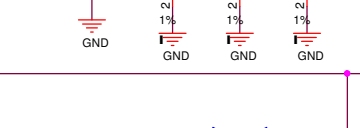
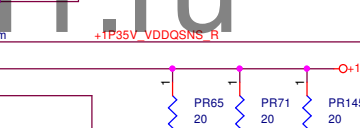
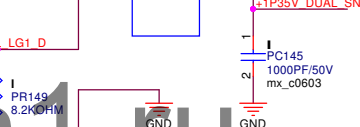
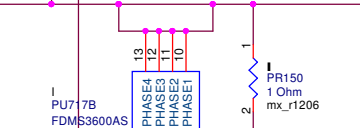
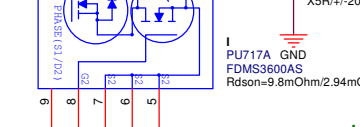
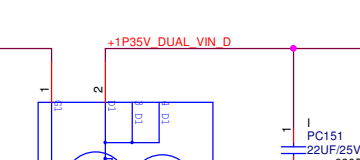
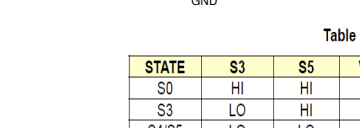
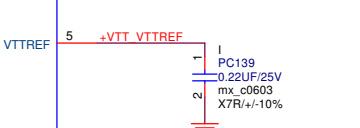
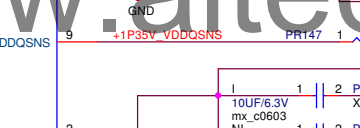
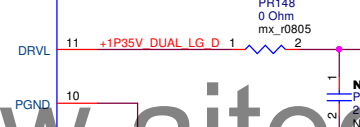
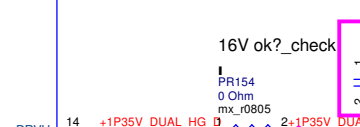
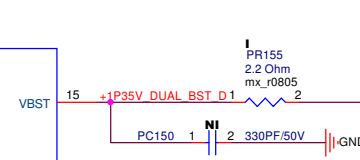
$$V_{trip} = R_{cs} * I_{cs}/8$$

$$R_{cs} = 29.4K \text{ ohm}$$

OCP=21.6A



GP_DDR_Vref	Vref
1	1.35
0	1.5



+1P35V_DUAL/ Max:11.795A / TDC:8.2565A

Fsw = 300kHz
Iin = 1.0479A
Delta I = 4.18A
ripple = 29.26mV
OCP = 21.6A
H/S = 0.599W
L/S = 0.882W

+0P675V_VTT/Imax=1.1A/TDC=0.77A

Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

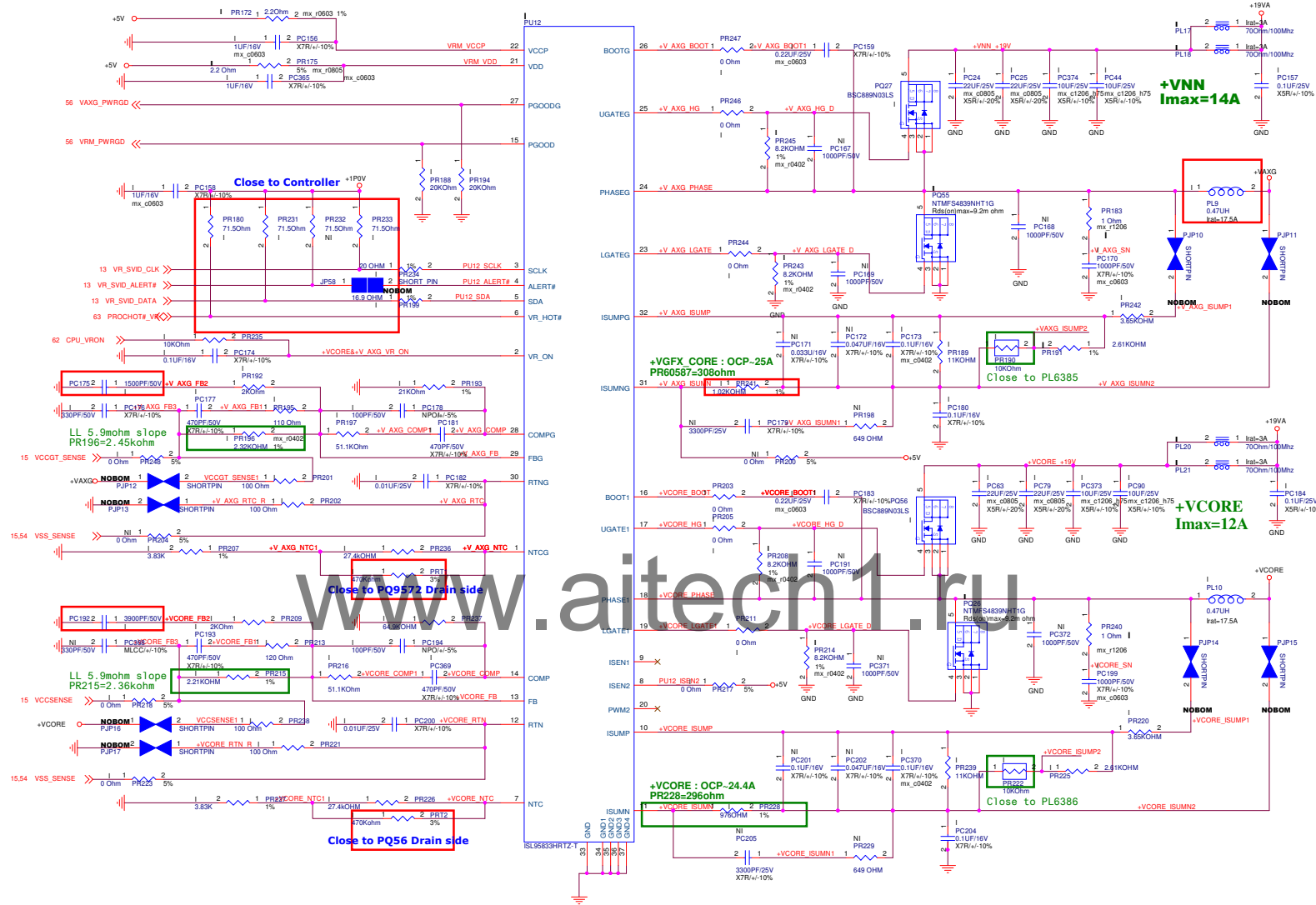
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +1P35V_DUAL&VTT_DDR

Engineer: Wade Pan

Size A3 Project Name IAXBT-BL Rev R1.01

Date: Tuesday, February 11, 2014 Sheet 53 of 67



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : Vcore Controller

PEGATRON Corp. Engineer: Wade_Pan

Size Project Name

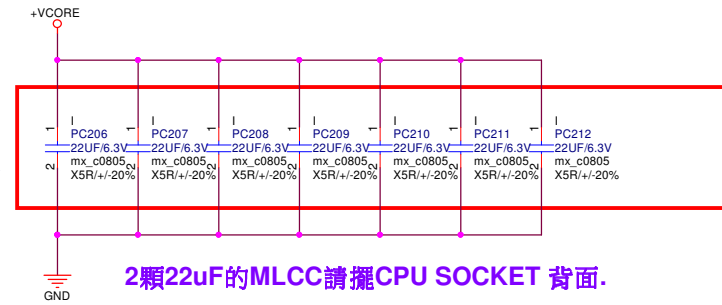
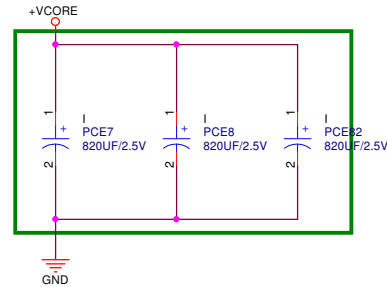
A2 IAXBT-BL Rev R1.01

Date: Tuesday, February 11, 2014 Sheet 54 of 67

VCORE OUTPUT CAP

PL-CAP *3
MLCC 22uF*7
10uF*0
4.7uF*0
2.2uF*0

靠近CPU SOCKET for transient

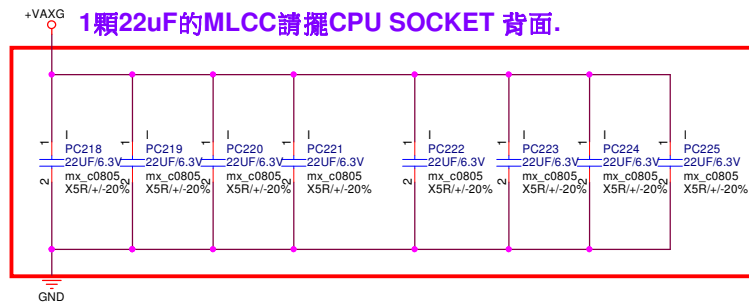
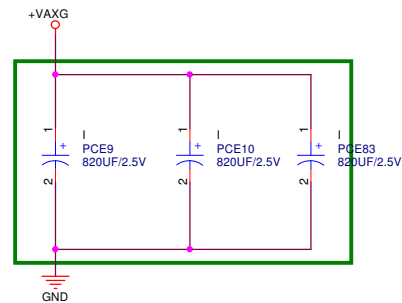


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+VNN OUTPUT CAP

PL-CAP *3
MLCC 22uF*8
10uF*0
1uF*0

靠近CPU SOCKET for transient



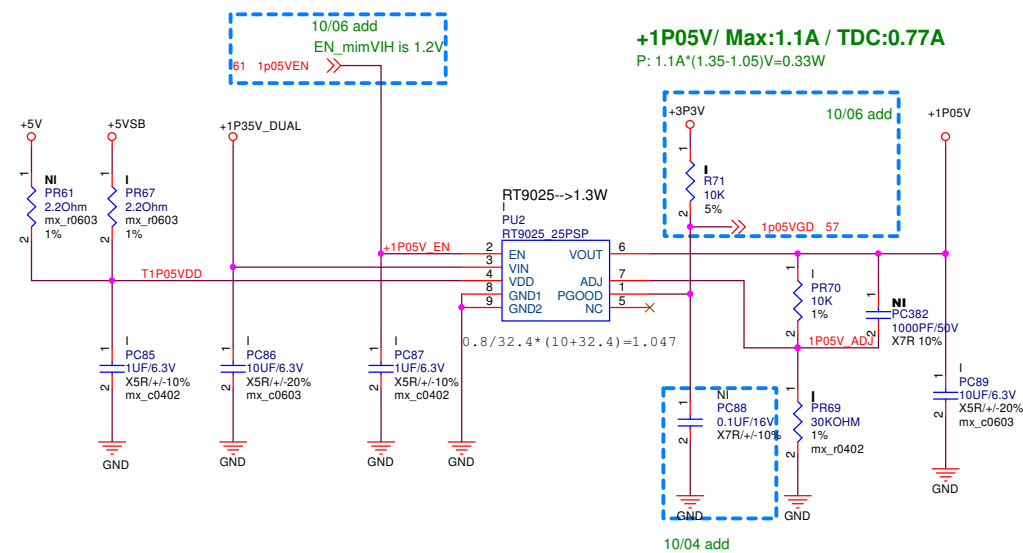
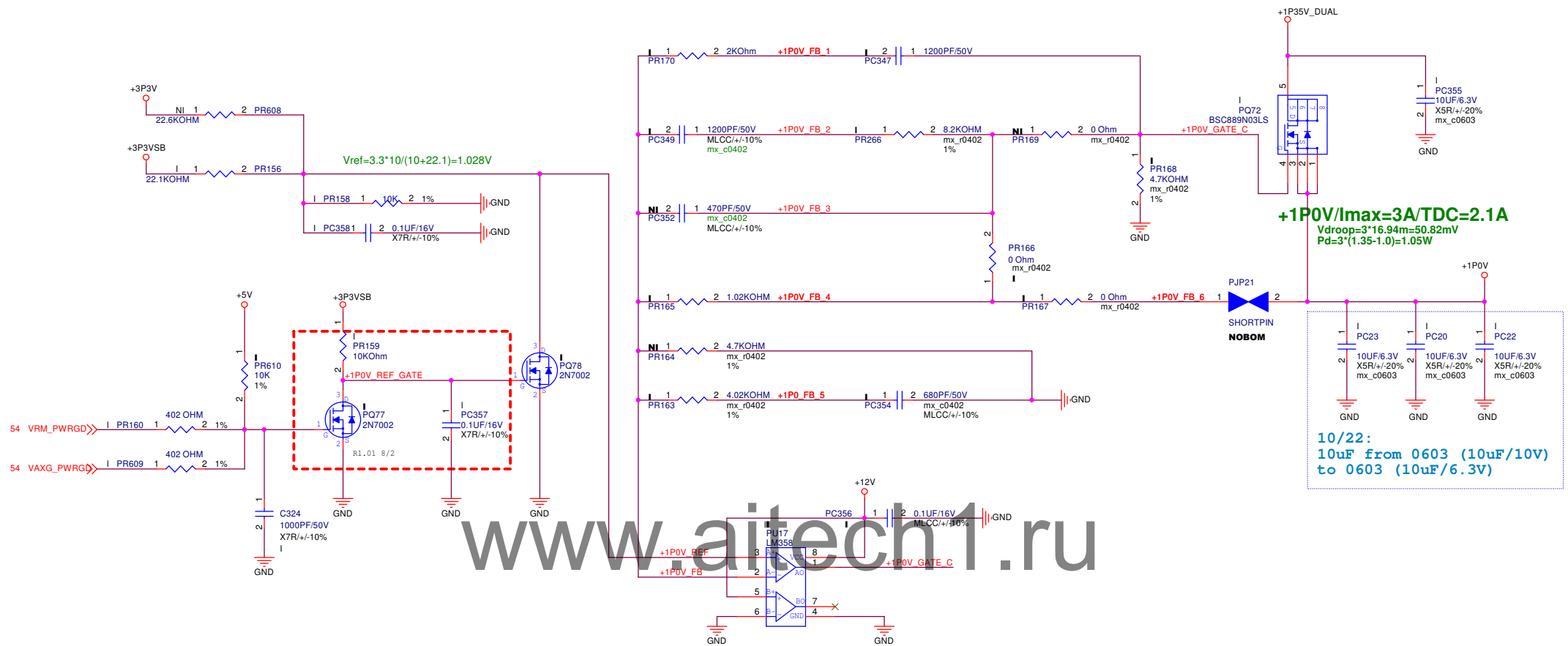
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +Vcore & +VNN Output

Pegatron Corp. Engineer: Wade_Pan

Size A3	Project Name IAXB-T-BL	Rev R1.01
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Date: Tuesday, February 11, 2014 Sheet 55 of 67



PEGATRON DT-MB RESTRICTED SECRET

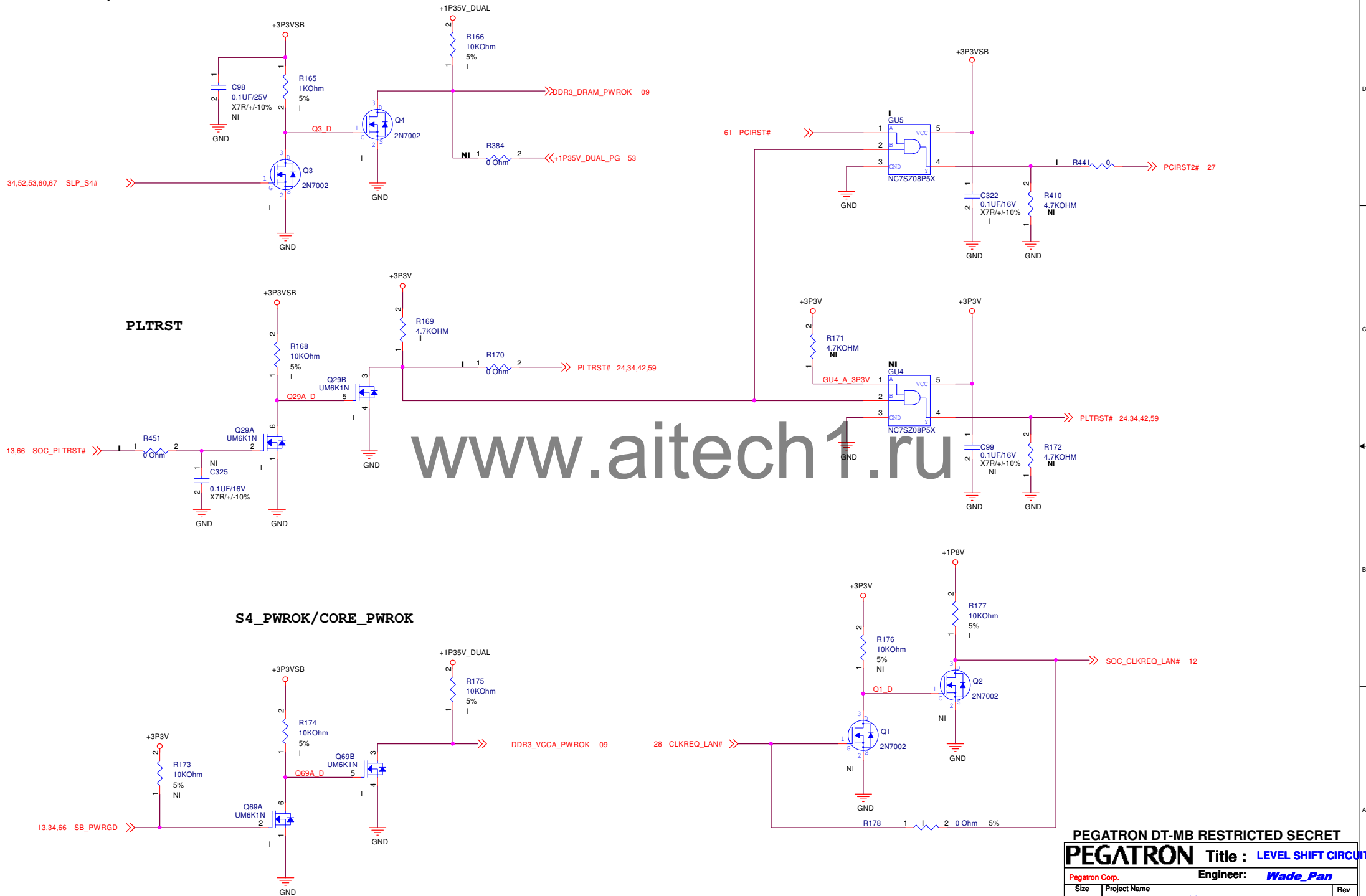
PEGATRON Title: **1P0V_1P05V**

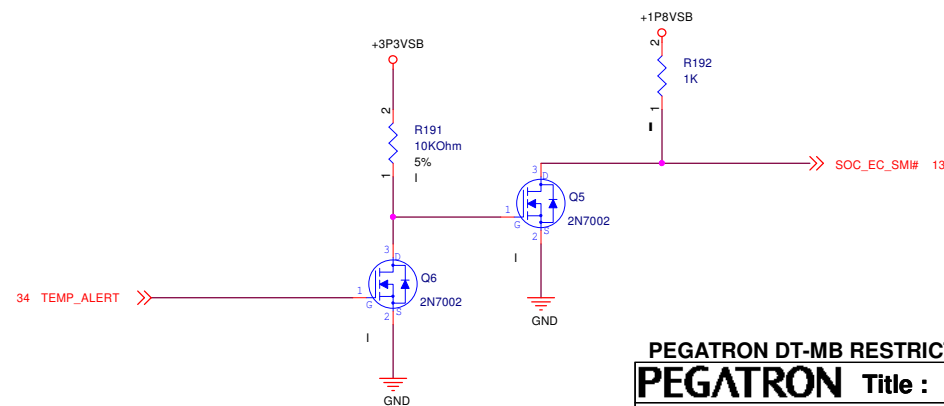
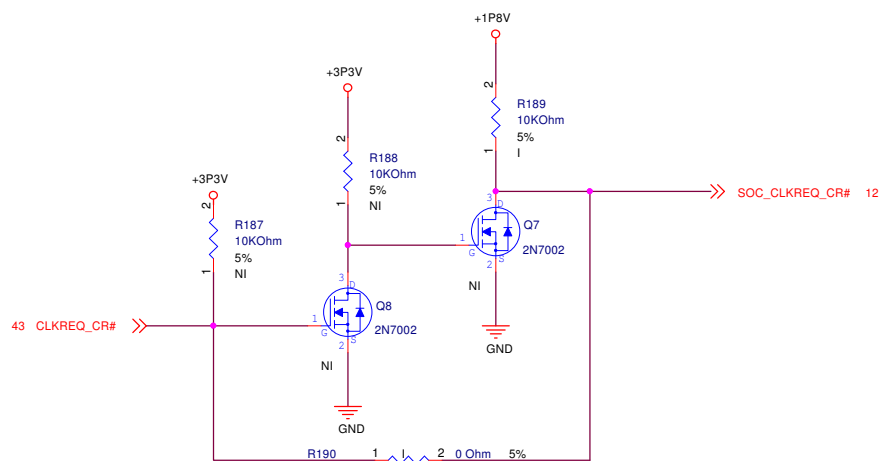
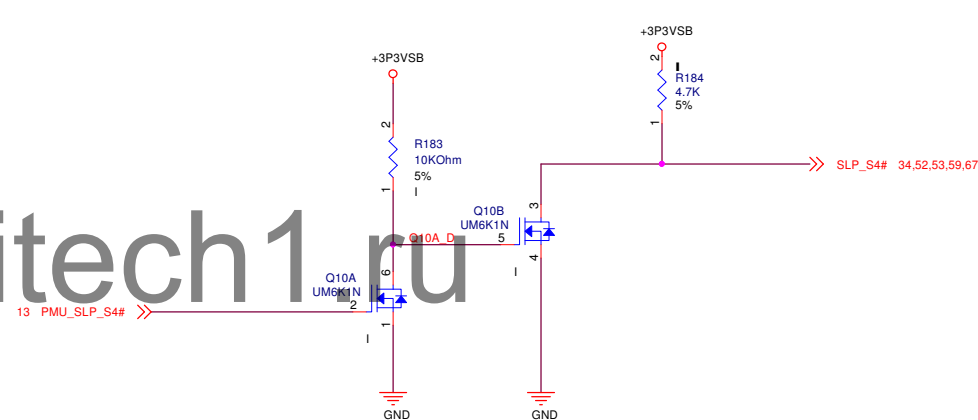
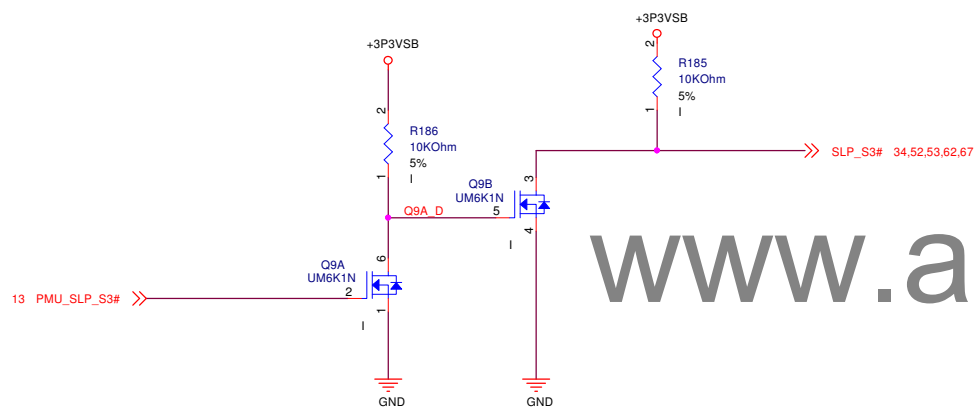
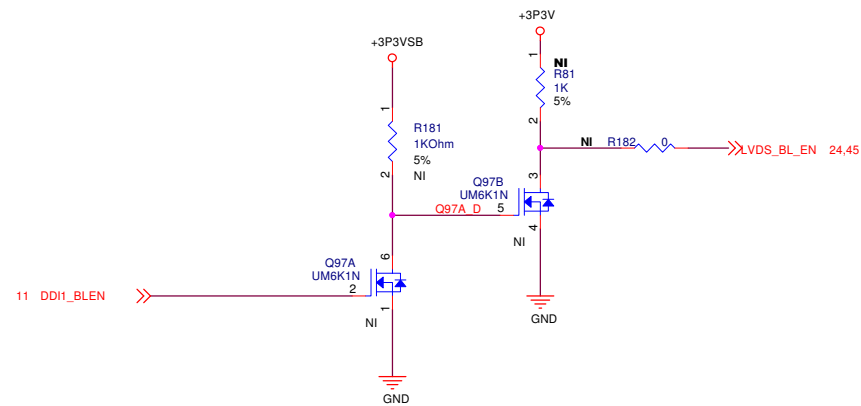
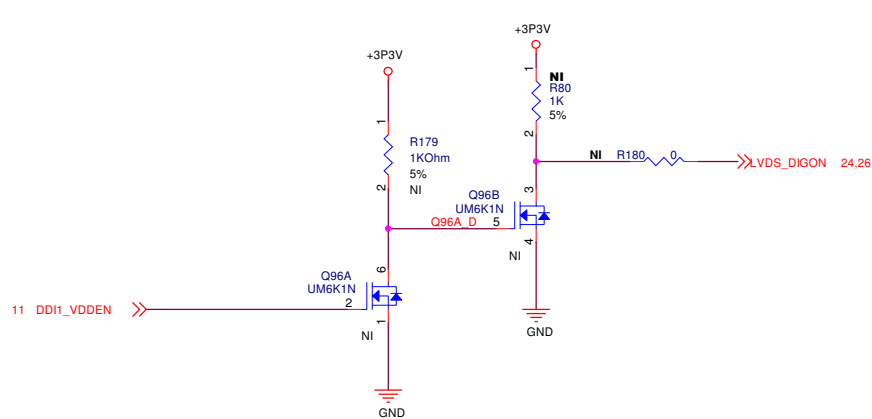
Pegatron Corp. Engineer: **Wade_Pan**

Size	Project Name	Rev
A3	IAXBT-BL	R1.01

Date: Tuesday, February 11, 2014 Sheet 56 of 67

BUFFER/LEVEL SHIFT





34 TEMP_ALERT

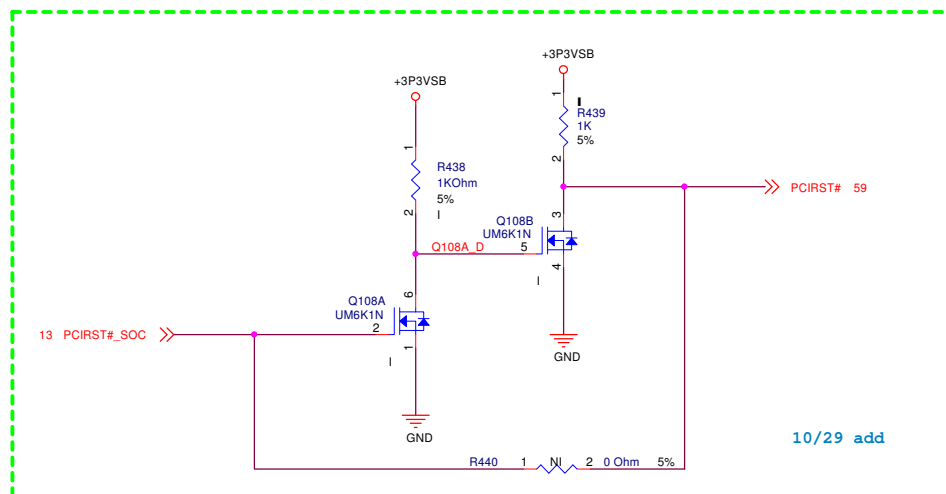
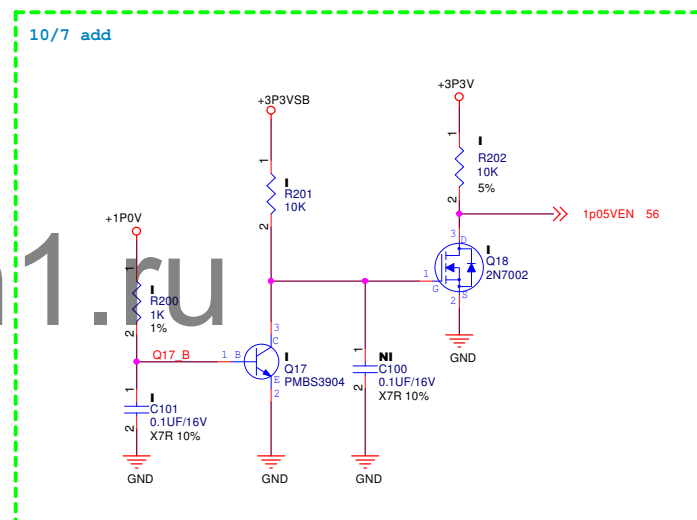
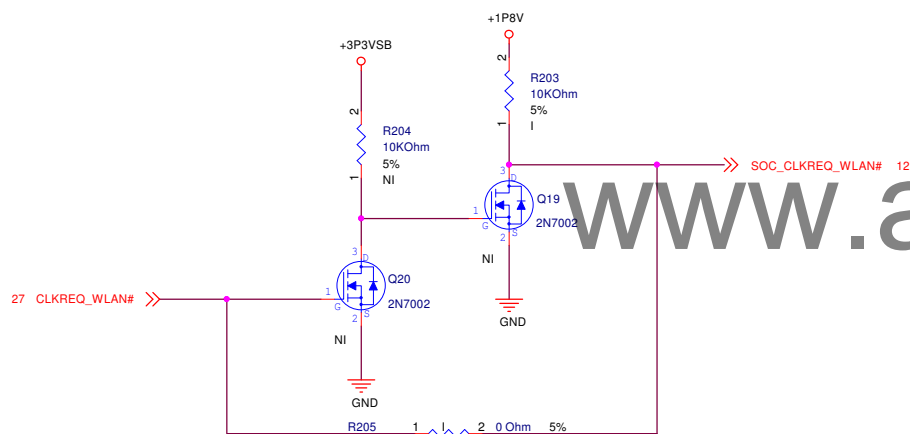
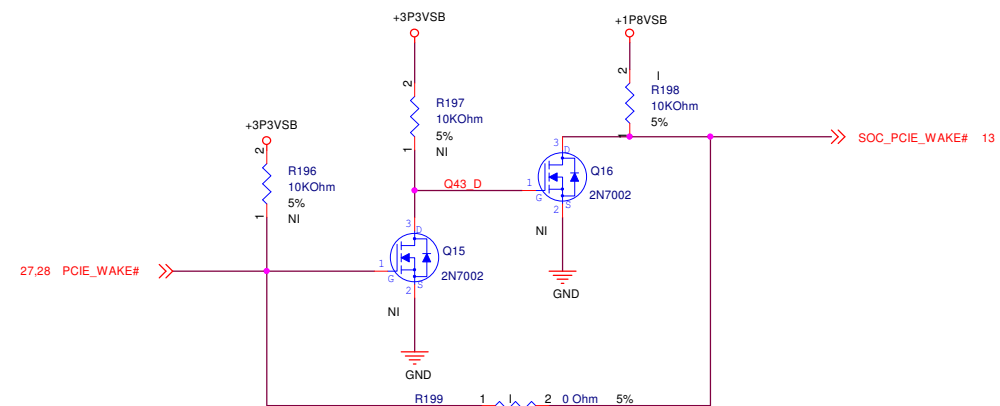
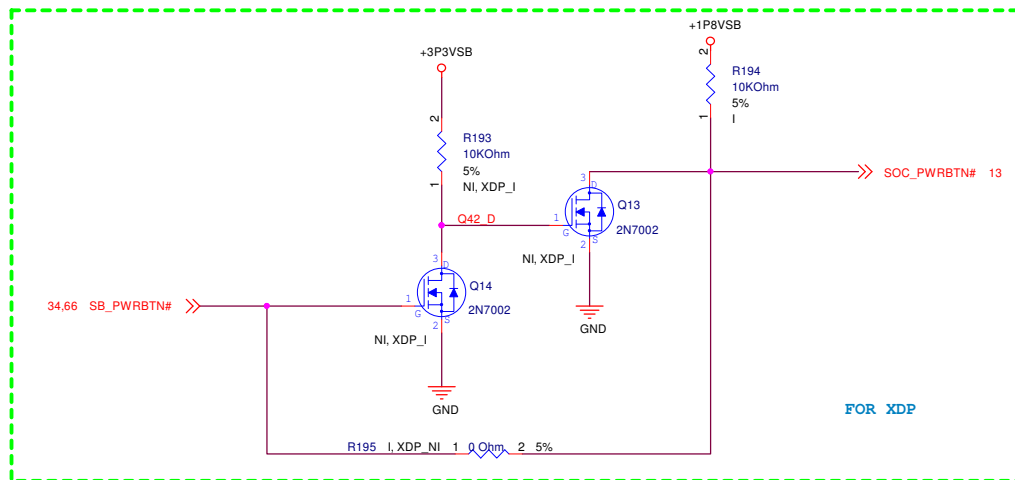
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : LEVEL SHIFT CIRCUIT & ST

Pegatron Corp. Engineer: **Wade Pan**

Size A3 Project Name **IAXBT-BL** Rev R1.01

Date: Tuesday, February 11, 2014 Sheet 60 of 67



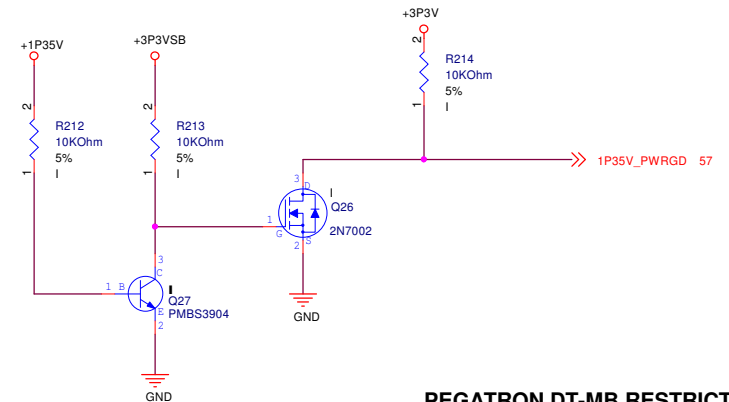
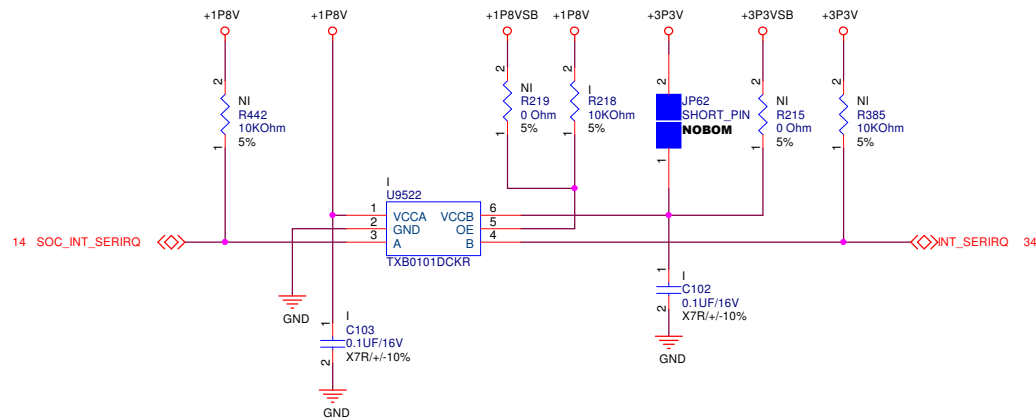
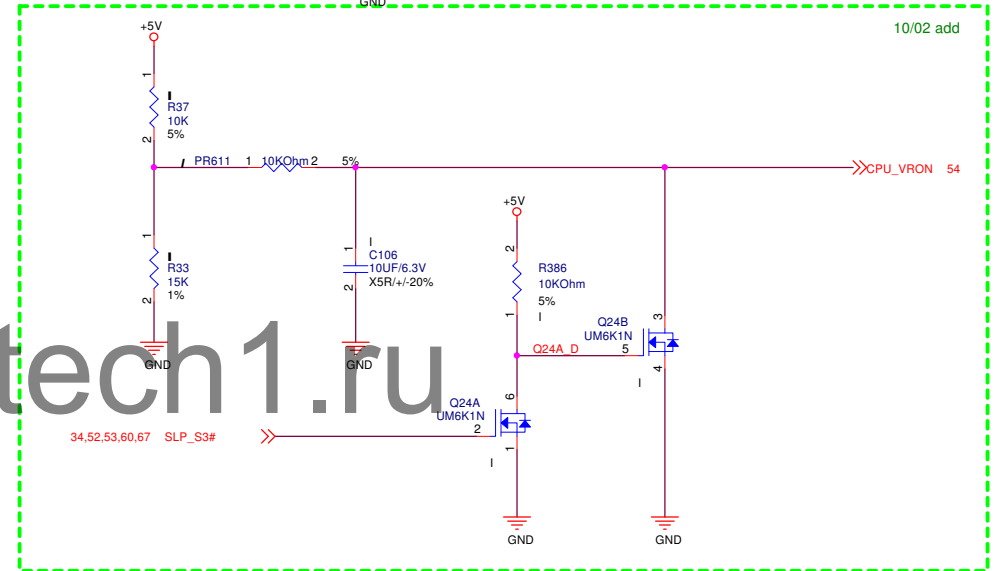
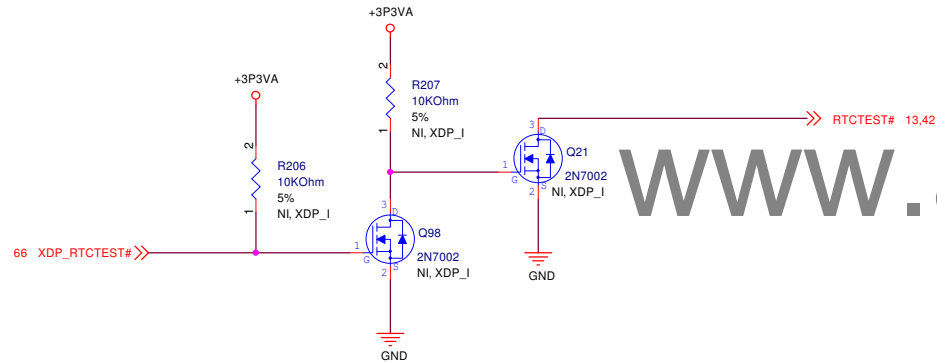
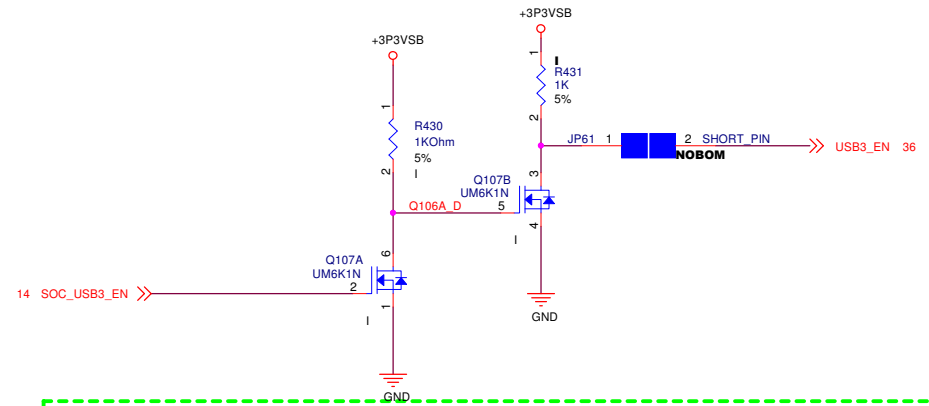
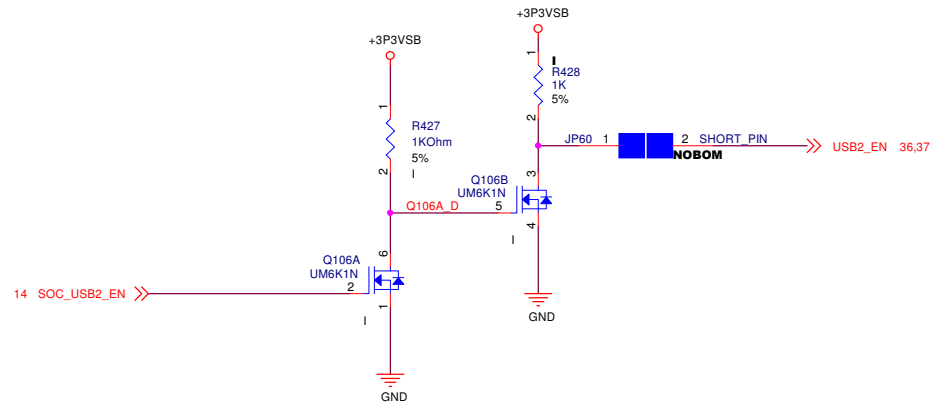
PEGATRON DT-MB RESTRICTED SECRET

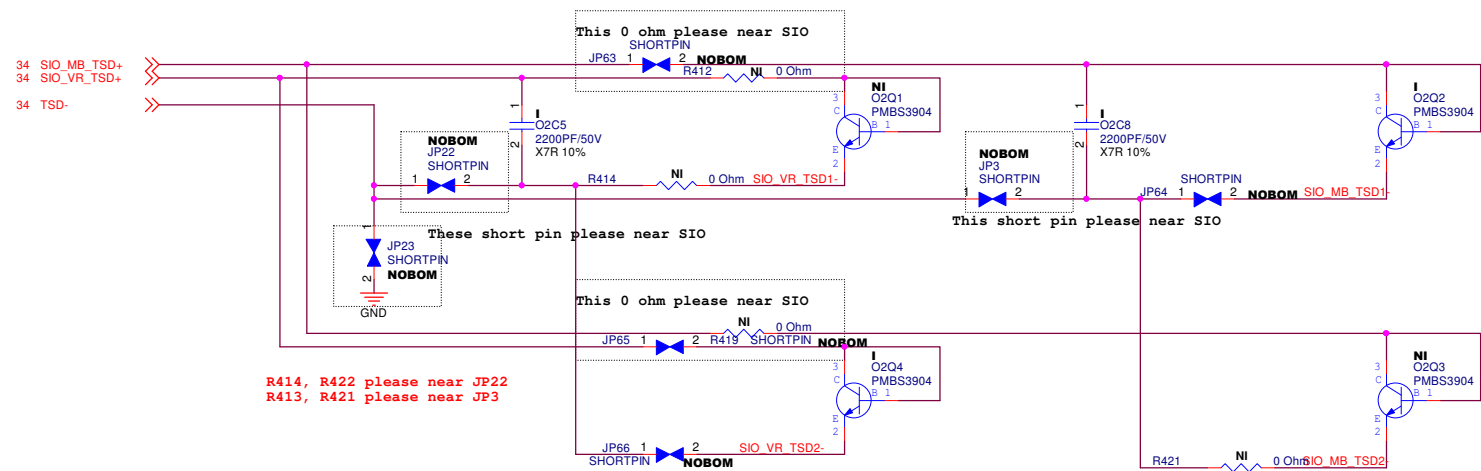
PEGATRON Title : LEVEL SHIFT CIRCUIT & ST

Pegatron Corp. Engineer: Wade Pan

Size A3 Project Name IAXBT-BL Rev R1.01

Date: Tuesday, February 11, 2014 Sheet 61 of 67



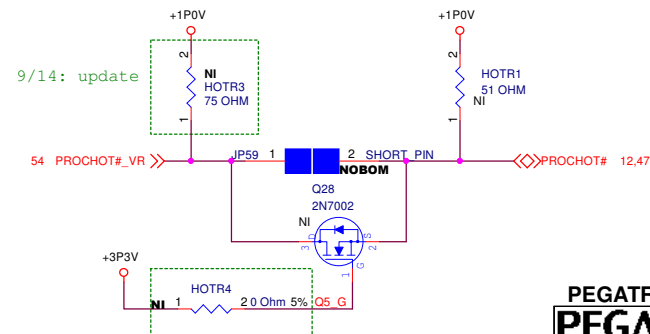
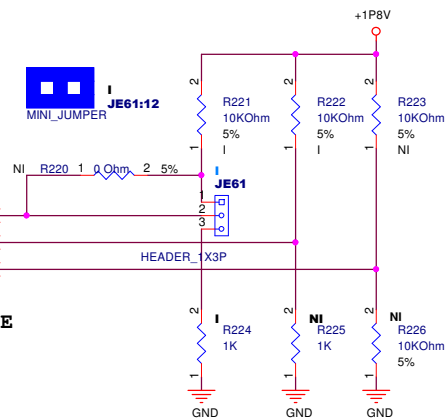


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NOTE .

GPIO_S0_SC65==> SECURITY FLASH DESCRIPTORS
 GPIO_S0_SC63==> BIOS BOOT SELECTION
 GPIO_S0_NC13==> DDI1 DETECT

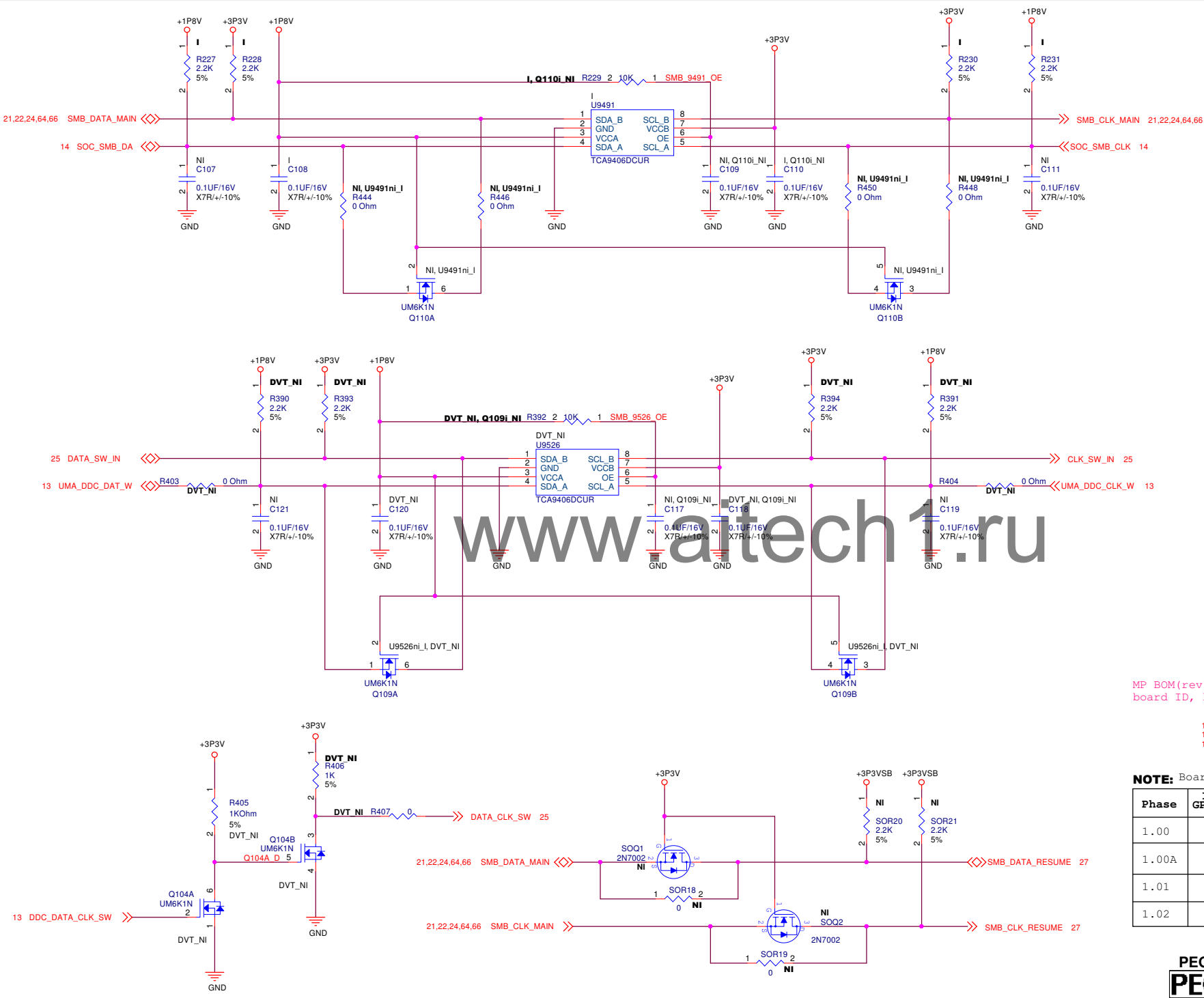
ALL RESISTORS AS CLOSED TO SOC AS POSSIBLE



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : LEVEL SHIFT CIRCUIT & ST

Size	Project Name	Engineer:	Rev
A3	IAXBT-BL	Wade_Pan	R1.01
Date:	Tuesday, February 11, 2014	Sheet	63 of 67

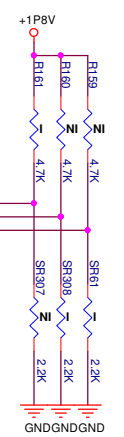


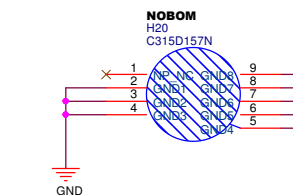
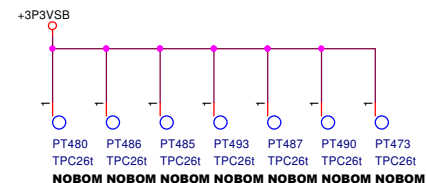
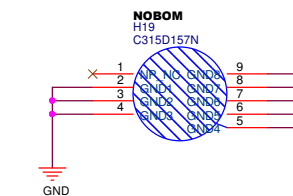
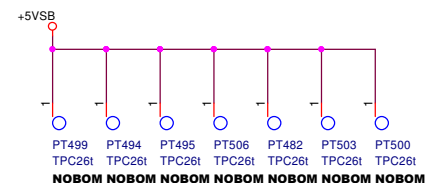
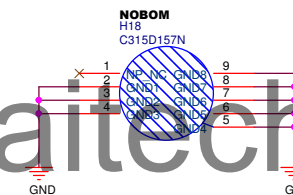
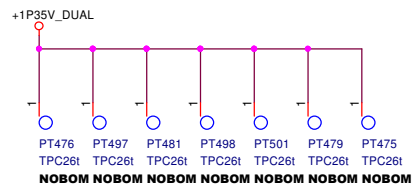
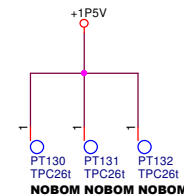
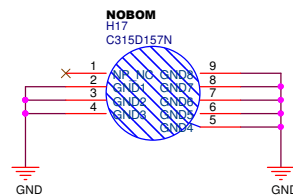
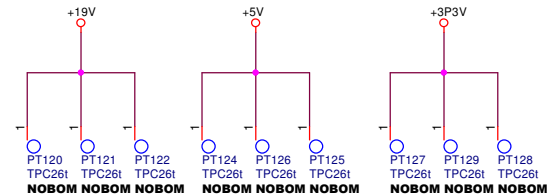
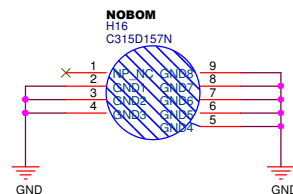
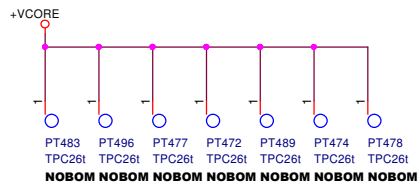
MP BOM(rev1.02) have not change board ID, keep 1.0.0

14 BRD_ID0
14 BRD_ID1
14 BRD_ID2

NOTE: Board ID Select

Phase	ID0 GPIO90	ID1 GPIO91	ID2 GPIO92
1.00	1	1	1
1.00A	--	--	--
1.01	1	0	0
1.02	--	--	--





0913 Update

